65V Input, 5A Output, Asynchronous Step-Down DC/DC Converter

FEATURES

- 4.8V to 65V Operating Input Range
- RY8650：5A Output Current
- 0.8V±1% Internal Voltage Reference
- Adjustable Soft Start
- UVLO/OTP/OCP Protections
- Package：DFN4×4-10 ESOP8
- RoHS Compliant and Halogen Free

APPLICATIONS

- Factory automation & control
- Vehicle Accessories: GPS Entertainment
- USB Dedicated Charging Ports and Battery Chargers
- 12-V, 24-V and 48-V Industrial, Automotive and Communications Power Systems

DESCRIPTION

The RY8650 achieves 5A of continuous output current from 4.8V to 65V input voltage. At light loads, it works in the discontinuous conduction mode (DCM) and can achieve high efficiency. In DCM mode, the inductor current will not reverse. The RY8650 module skips several cycles under low output load conditions. Current mode control provides tight load transient response and cycle-by-cycle current limit.

The RY8650 device is also guarantees robustness with output short protection, thermal protection and input under voltage lockout.

TYPICAL APPLICATION

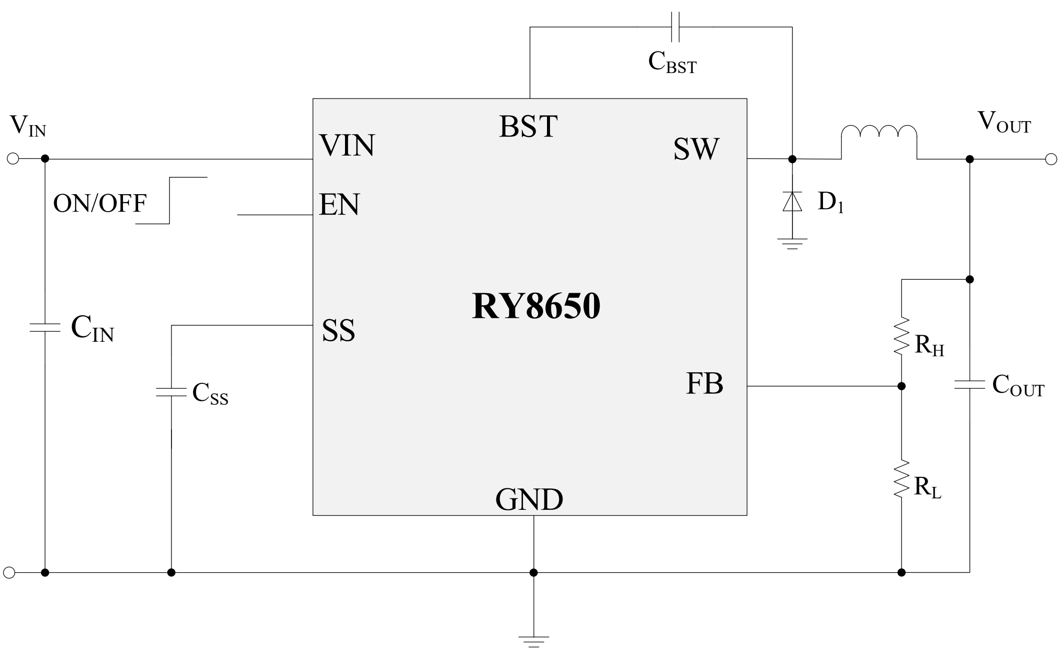
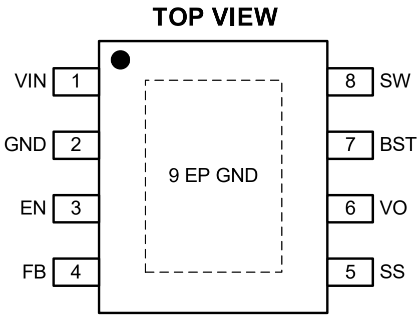


Figure 1. Schematic Diagram

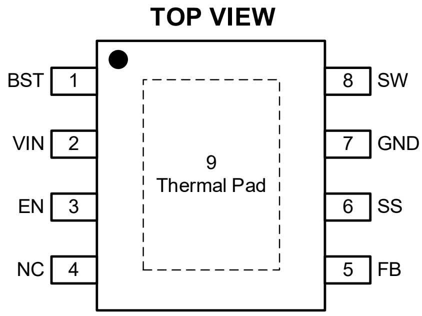
65V Input, 5A Output,
Asynchronous Step-Down DC/DC Converter

Pin Description

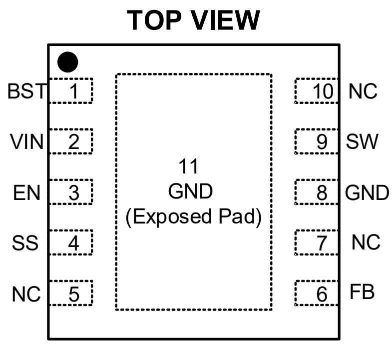
Pin Configuration



ESOP8(AP)



ESOP8(CP)



DFN10-4X4(CD)

Pin Definition

DFN10	ESOP8		Name	Pin Description
CD	BP	CP		
1	7	1	BST	Bootstrap pin for top switch. Connect a 0.1uF capacitor between BST and SW pin to supply current for the top switch driver.
2	1	2	VIN	Input pin. Connect a 4.8V to 65V supply to VIN and bypass VIN to GND with a suitably large capacitor to eliminate noise on the input to the IC.
3	3	3	EN	Enable pin. Pull high to enable the device. Pull low to disable the device. Do not leave it floating.
4	5	6	SS	Soft-start time setting pin. The soft-start time is determined by the capacitance between SS pin and GND.
6	4	5	FB	Output Feedback Pin. Connect this pin to the center point of the output resistor divider to program the output voltage: $V_{OUT}=0.8\times(1+R_H/R_L)$.
8	2	7	GND	Ground pin.
9	8	8	SW	SW is the switching node that supplies power to the output. Connect the output LC filter from SW to the output load.
	6		VO	Output Over-Voltage Protection. Connect VO to the tap of an external resistor divider from VOUT to GND. The OVP reference is 0.9V.
5,7,10		4,	NC	Not Connected.

11	9	9	Thermal Pad	GND pin must be electrically connected to the exposed pad on the printed circuit board for proper operation

Order Information

Marking	Part No.	Model	Description	Package
8650D YYLL	70301965	RY8650CD10	RY8650CD10, 5A Buck Asynchronous Step-Down DC/DC Converter, 4.8-65V, 5A, VFB 0.8V, DFN4x4-10	DFN4x4-10
8650P YYLL	70301808	RY8650AP8	RY8650AP8, 5A Buck Asynchronous Step-Down DC/DC Converter, 4.8-65V, 5A, VFB 0.8V, ESOP8	ESOP8
8650C YYLL	70301970	RY8650CP8	RY8650CP8, 5A Buck Asynchronous Step-Down DC/DC Converter, 4.8-65V, 5A, VFB 0.8V, ESOP8	ESOP8

Specifications

Absolute Maximum Ratings (1) (2)

Item	Min	Max	Units
VIN	-0.3	65	V
SW	-0.6V (-7V for 10ns)	72V (74V for 20ns)	V
BST	SW-0.3V	SW+6V	V
EN	-0.3	8.4	V
SS	-0.3	3	V
All Other Pin	-0.3	6	V
Junction Temperature	-40	150	ºC
Lead Temperature(Soldering, 10 sec.)	——	260	ºC
Storage Temperature Range	-55	150	ºC
ESD Susceptibility (Human Body Model).	——	2	kV
ESD Susceptibility (Charged Device Model).	——	500	V

Note (1): Exceeding these ratings may damage the device.

Note (2): The device is not guaranteed to function outside of its operating conditions.

Recommended Operating Conditions

Item	Min	Max	Units
V_{IN}	4.8	65	V
V_{OUT}	0.8V	Dmax*V_{IN}	A
T_J(Junction Temperature Range)	-40	125	ºC
T_A(Operating Ambient Temperature）(1)	-40	85	ºC

Note (1): All limits specified at room temperature (TA = 25°C) unless otherwise specified. All room temperature limits are 100% production tested. All limits at temperature extremes are ensured through correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).

Thermal Information

Item	Description	DFN4×4-10	ESOP8	Unit
$R_{\theta JA}$	Junction-to-ambient thermal resistance (1)(2)	36	42.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	31.9	56.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	13.2	25.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	9.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	13.5	25.4	°C/W
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	3	3.8	°C/W

Note (1): The package thermal impedance is calculated in accordance to JESD 51-7.

Note (2): Thermal Resistances were simulated on a 4-layer, JEDEC board

Electrical Characteristics (1)(2)

(V_{IN} = 12V, T_A= -40~125°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Specifications						
Input Voltage Range	V_{IN}		4.8		65	V
Input UVLO Threshold (rising)	V_{UVLO},rising	EN=V_{IN}		4.4		V
Input UVLO Threshold (falling)	V_{UVLO},falling	EN=V_{IN}		4.2		V
Input UVLO Hysteresis	V_{HYS}			200		mV
Supply Current	I_Q	V_{EN}=5V, V_{FB}=1V		180		µA
Shutdown Supply Current	I_{SD}	V_{EN}=0V, Tj=+25℃		4		µA
Output Specifications						
Feedback Reference Voltage	V_{FB}	4.8V≤VIN≤65V	792	800	808	mV
Top Switch Resistance	$R_{DS(ON)}$			97		mΩ
Power Switch Leakage Current	ILEAK	V_{IN}=65V,VEN=0V, VSW=0V@25C			6	µA
Current Limit	I_{LIM}			7.2		A
Soft-Start Charge Current	I_{SS}			1.8		µA
Minimum On Time[4]	TON_MIN			100		ns
Minimum Off-Time	TOFF_MIN			165		ns
General Specifications						
Switching Frequency	f_{SW}	RRT=200k		350		kHz
Thermal Shutdown Temperature	T_{TSD}			150		°C
Thermal Shutdown Hysteresis	T_{TSD_HYST}			20		°C
Signal Specifications						
EN Rising Threshold	V_{EN_H}	V_{EN} rising, FB=0.6V		1.22		V
EN Falling Threshold	V_{EN_L}	V_{EN} falling, FB=0.3V		1.12		V
Thermal Shutdown[4]	T_{TSD}			170		℃
Thermal Shutdown hysteresis[4]	T_{TSD_HYST}			20		℃

Note (1): MOSFET on-resistance specifications are guaranteed by correlation to wafer level measurements.

Note (2): Thermal shutdown specifications are guaranteed by correlation to the design and characteristics analysis.

Typical Performance Characteristics (5)(6)(7)

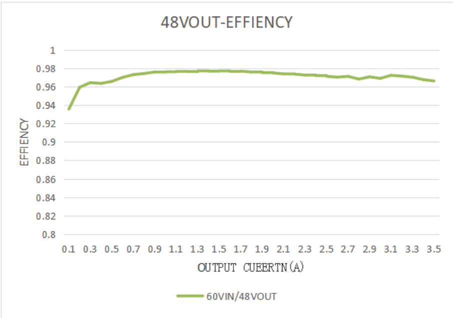
Note (5): Performance waveforms are tested on the evaluation board.

Note (6):C_{SS}=10nF, R_T=240kΩ, C_{BST}=100nF, T_A = +25ºC, C_{SS}=100nF, Cout=10uF*5， unless otherwise noted.

Note (7):In the environment below 1m/s and 55ºC, the 12V output current is less than or equal to 4A;the 24V output current is less than or equal to 3A.

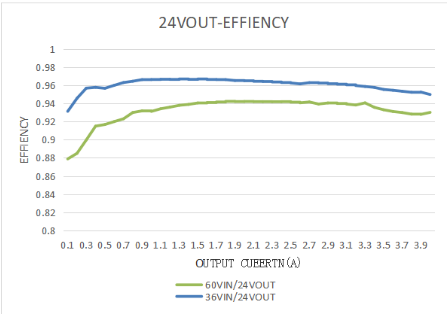
Efficiency vs Load Current

V_{OUT}=48V, L=33uH



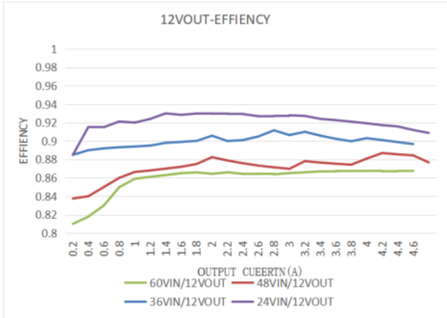
Efficiency vs Load Current

V_{OUT}=24V, L=22uH



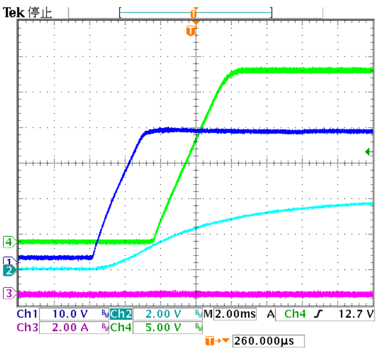
Efficiency vs Load Current

V_{OUT}=12V, L=6.8uH



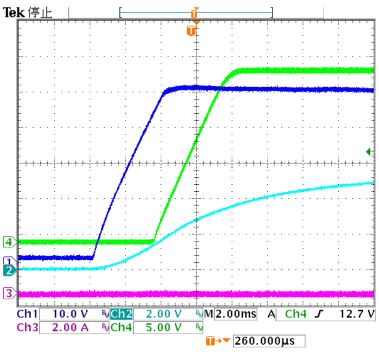
Power Up at No Load

V_{IN}=36V, V_{OUT}=24V, I_{OUT}=0A,L=22uH



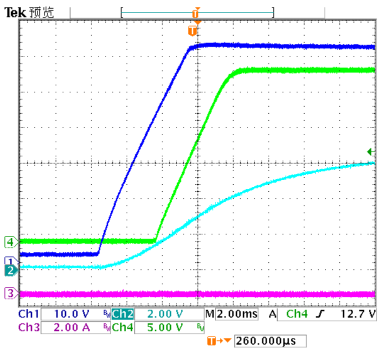
Power Up at No Load

V_{IN}=48V, V_{OUT}=24V, I_{OUT}=0A,L=22uH



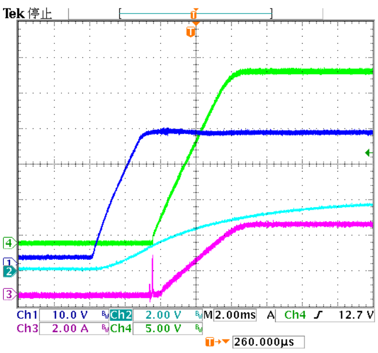
Power Up at No Load

V_{IN}=60V, V_{OUT}=24V, I_{OUT}=0A,L=22uH



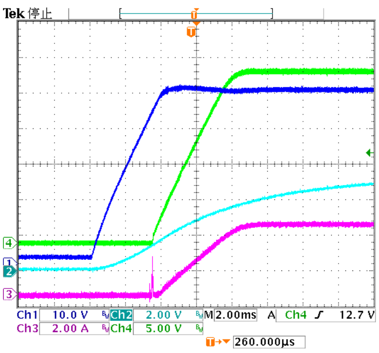
Power Up at Full Load

V_{IN}=36V, V_{OUT}=24V, I_{OUT}=4A,L=22uH



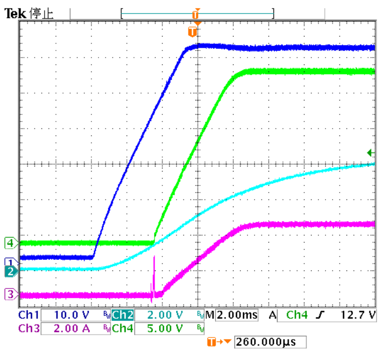
Power Up at Full Load

V_{IN}=48V, V_{OUT}=24V, I_{OUT}=4A,L=22uH



Power Up at Full Load

V_{IN}=60V, V_{OUT}=24V, I_{OUT}=4A,L=22uH



Power Down at No Load

V_{IN}=36V, V_{OUT}=24V, I_{OUT}=0A,L=22uH

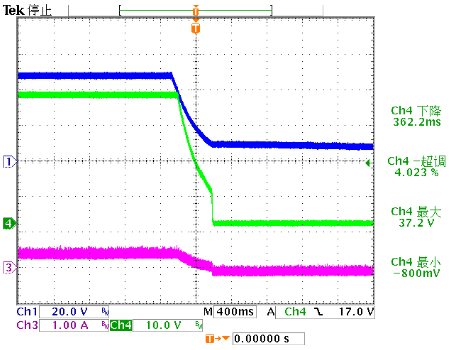
Power Down at No Load

V_{IN}=48V, V_{OUT}=24V, I_{OUT}=0A,L=22uH

Power Down at No Load

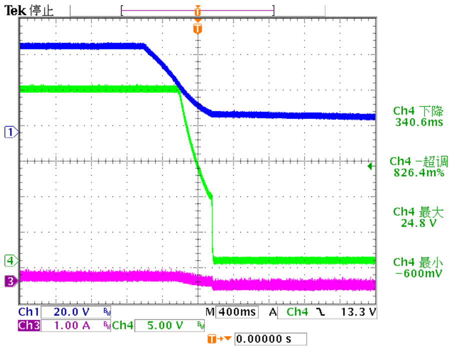
V_{IN}=60V, V_{OUT}=24V, I_{OUT}=0A,L=22uH

65V Input, 5A Output, Asynchronous Step-Down DC/DC Converter



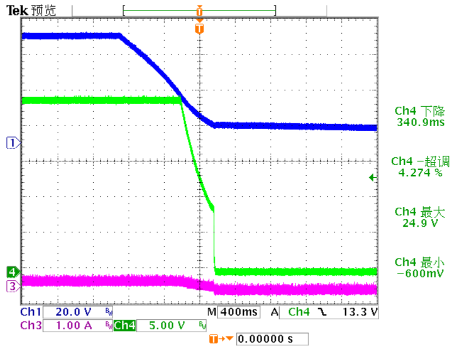
Power Down at Full Load

V_{IN}=36V, V_{OUT}=24V, I_{OUT}=4A,L=22uH



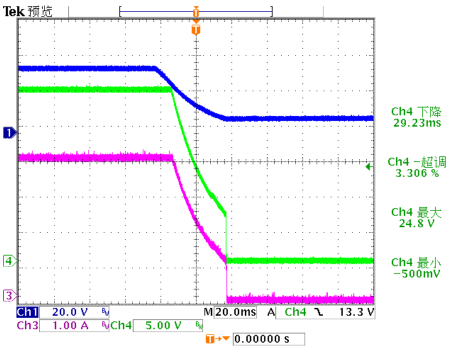
Power Down at Full Load

V_{IN}=48V, V_{OUT}=24V, I_{OUT}=4A,L=22uH



Power Down at Full Load

V_{IN}=60V, V_{OUT}=24V, I_{OUT}=4A,L=22uH



Enable Startup at No Load

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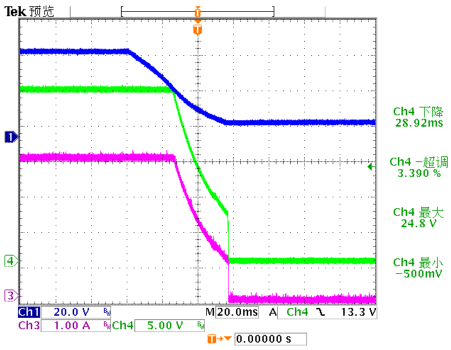
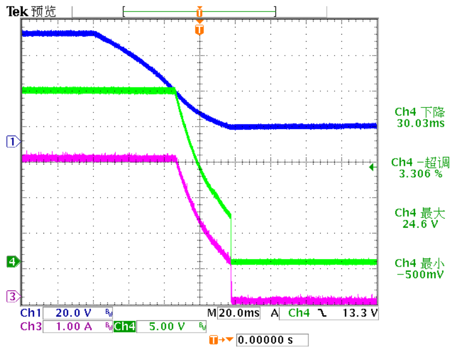


Enable Startup at No Load

V_{IN}=48V, V_{OUT}=24V, I_{OUT}=0A,L=22uH



Enable Shutdown No Load

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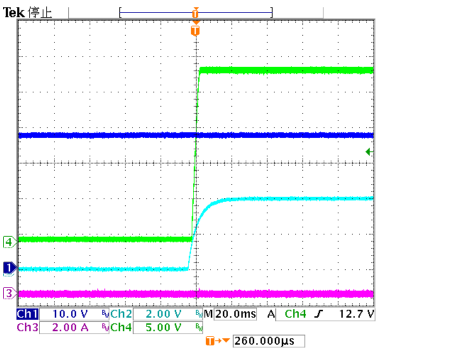
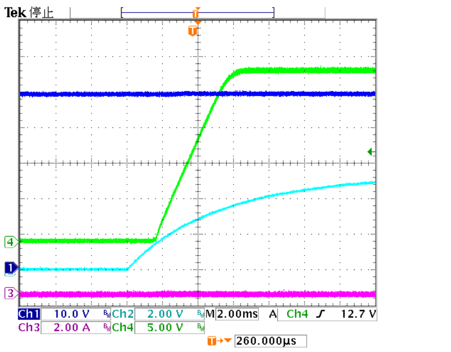


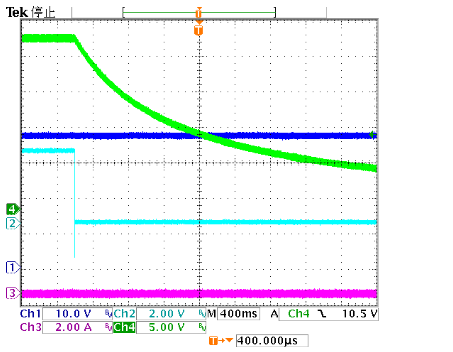
Enable Startup at Full Load

V_{IN}=36V, V_{OUT}=24V, I_{OUT}=4A,L=22uH



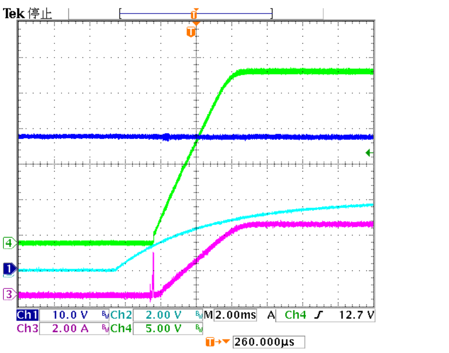
Enable Startup at Full Load

V_{IN}=48V, V_{OUT}=24V, I_{OUT}=4A,L=22uH

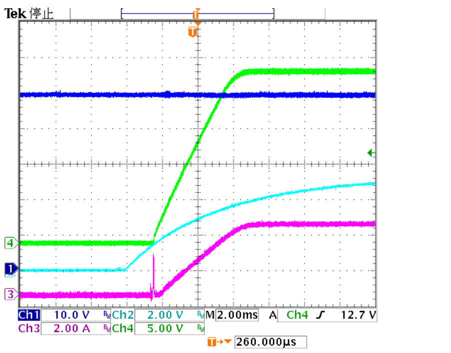


Enable Shutdown at Full Load

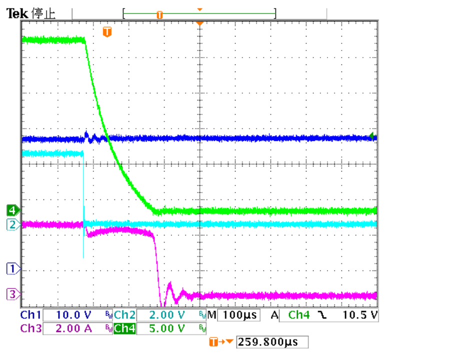
V_{IN}=36V, V_{OUT}=24V, I_{OUT}=4A,L=22uH



Output Ripple Voltage



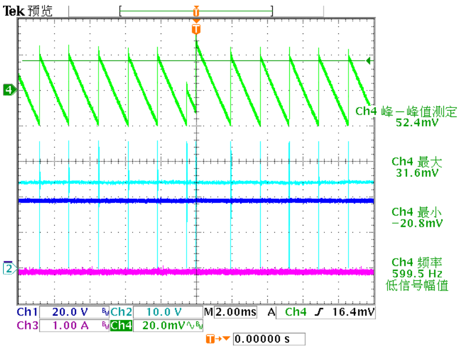
Output Ripple Voltage



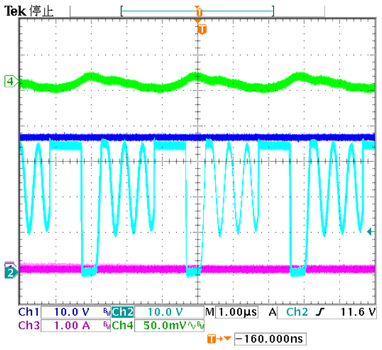
Output Ripple Voltage

65V Input, 5A Output, Asynchronous Step-Down DC/DC Converter

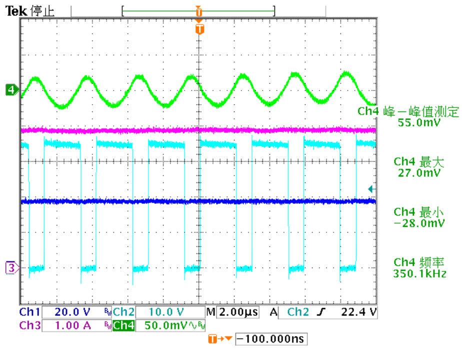
V_{IN}=36V, V_{OUT}=24V, I_{OUT}=0A,L=22uH



V_{IN}=36V, V_{OUT}=24V, I_{OUT}=0.5A,L=22uH

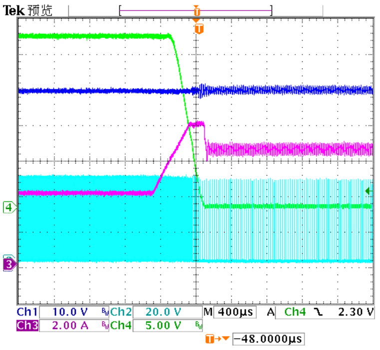


V_{IN}=36V, V_{OUT}=24V, I_{OUT}=4A,L=22uH



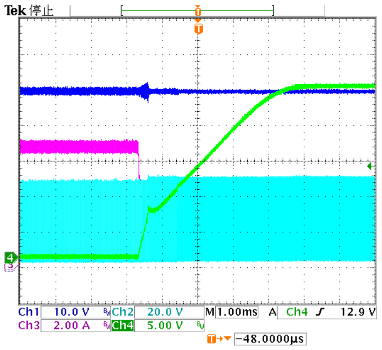
Over current Protection-Response

V_{IN}=36V, V_{OUT}=24V, L=22uH, I_{OUT}=4A to 8A



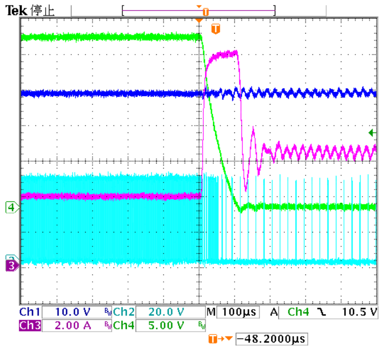
Over current Protection-Recovery

V_{IN}=36V, V_{OUT}=24V, L=22uH, I_{OUT}=8A to 0A



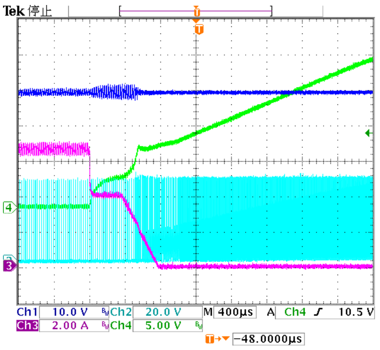
Short Circuit Entry

V_{IN}=36V, V_{OUT}=24V, L=22uH, I_{OUT}=4A to short



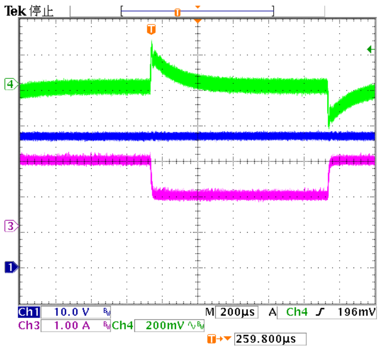
Short Circuit Recovery

V_{IN}=36V, V_{OUT}=24V, L=22uH, I_{OUT}=short to 0A



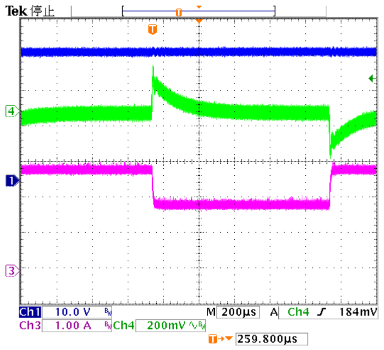
Loop Response

V_{IN}=36V, V_{OUT}=24V, L=22uH, I_{OUT}=1A-2A



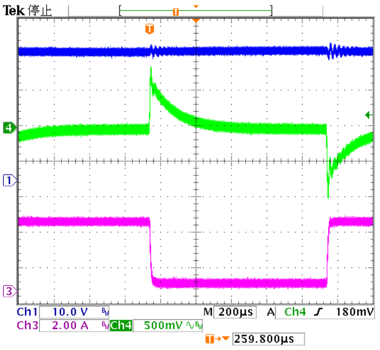
Loop Response

V_{IN}=36V, V_{OUT}=24V, L=22uH, I_{OUT}=2A-3A



Loop Response

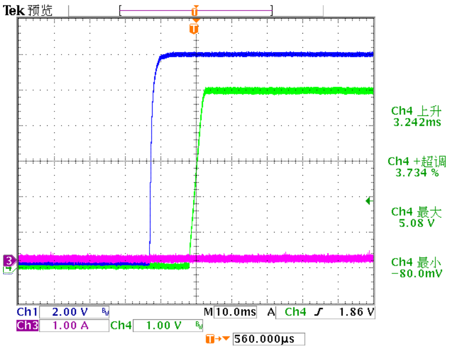
V_{IN}=36V, V_{OUT}=24V, L=22uH, I_{OUT}=2A-3A



65V Input, 5A Output, Asynchronous Step-Down DC/DC Converter

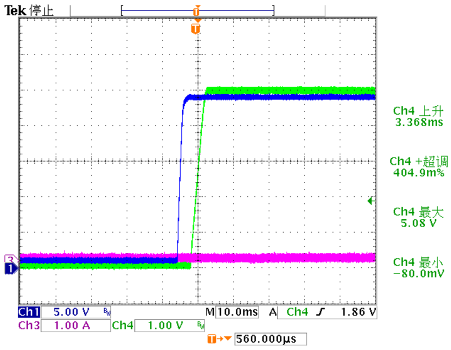
Power Up at No Load

V_{IN}=12V, V_{OUT}=5V, I_{OUT}=0A,L=6.8uH



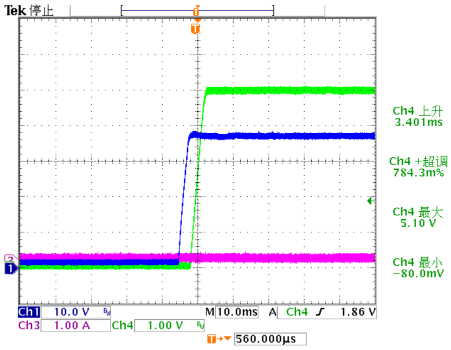
Power Up at No Load

V_{IN}=24V, V_{OUT}=5V, I_{OUT}=0A,L=6.8uH



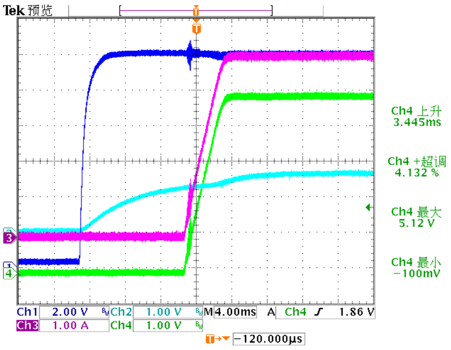
Power Up at No Load

V_{IN}=36V, V_{OUT}=5V, I_{OUT}=0A,L=6.8uH



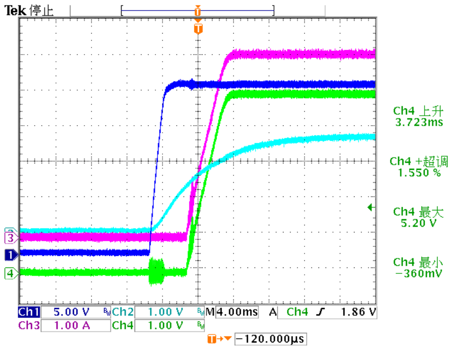
Power Up at Full Load

V_{IN}=12V, V_{OUT}=5V, I_{OUT}=5A,L=6.8uH



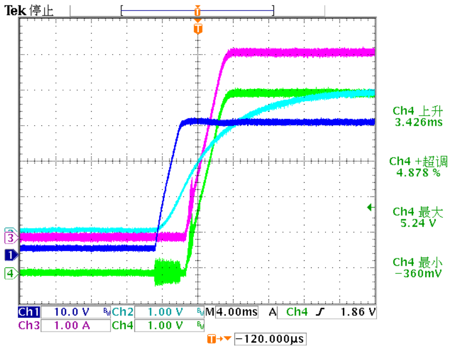
Power Up at Full Load

V_{IN}=24V, V_{OUT}=5V, I_{OUT}=5A,L=6.8uH



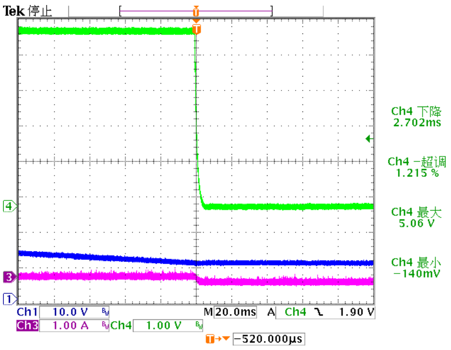
Power Up at Full Load

V_{IN}=36V, V_{OUT}=5V, I_{OUT}=5A,L=6.8uH



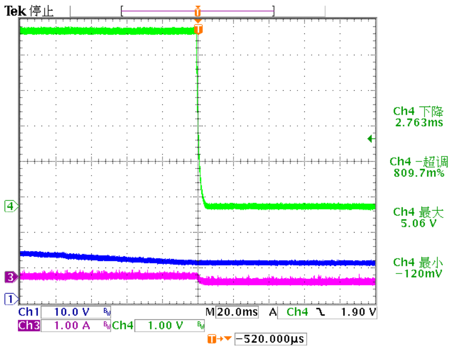
Power Down at No Load

V_{IN}=12V, V_{OUT}=5V, I_{OUT}=0A,L=6.8uH



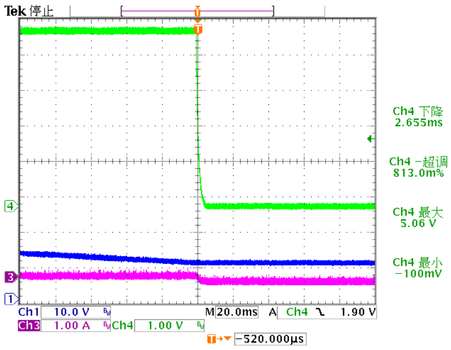
Power Down at No Load

V_{IN}=24V, V_{OUT}=5V, I_{OUT}=0A,L=6.8uH



Power Down at No Load

V_{IN}=36V, V_{OUT}=5V, I_{OUT}=0A,L=6.8uH



Power Down at Full Load

V_{IN}=12V, V_{OUT}=5V, I_{OUT}=5A,L=6.8uH

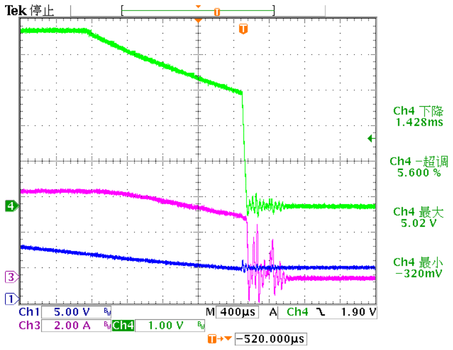
Power Down at Full Load

V_{IN}=24V, V_{OUT}=5V, I_{OUT}=5A,L=6.8uH

Power Down at Full Load

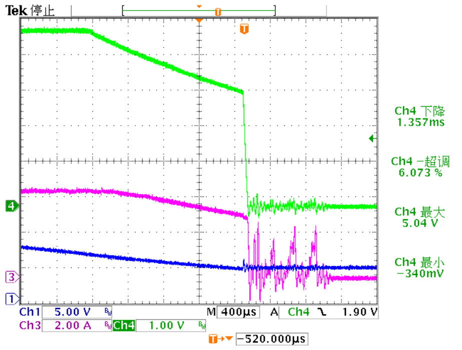
V_{IN}=36V, V_{OUT}=5V, I_{OUT}=5A,L=6.8uH

65V Input, 5A Output, Asynchronous Step-Down DC/DC Converter



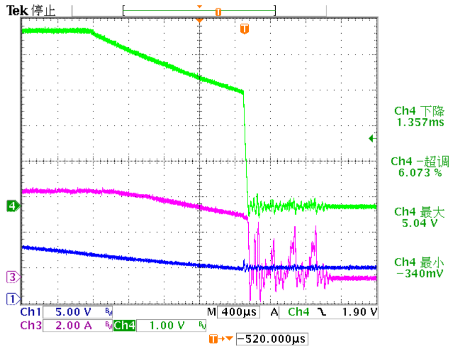
Output Ripple Voltage

V_{IN}=12V, V_{OUT}=5V, I_{OUT}=0A,L=6.8uH



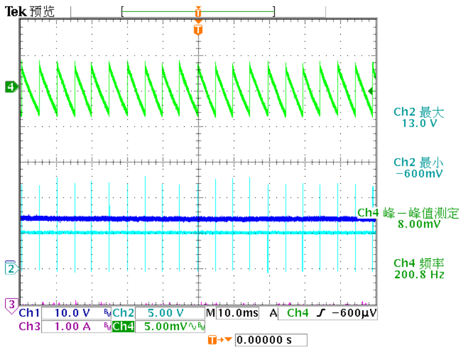
Output Ripple Voltage

V_{IN}=12V, V_{OUT}=5V, I_{OUT}=5A,L=6.8uH



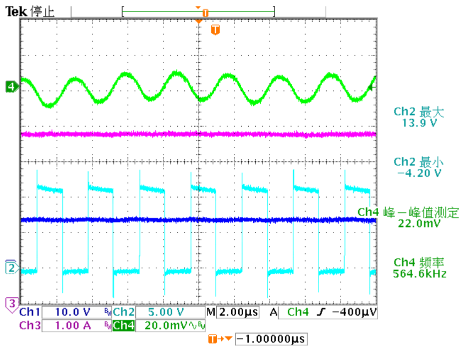
Output Ripple Voltage

V_{IN}=24V, V_{OUT}=5V, I_{OUT}=0A,L=6.8uH



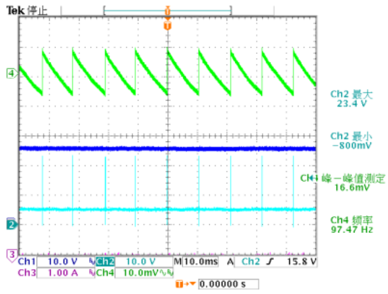
Output Ripple Voltage

V_{IN}=24V, V_{OUT}=5V, I_{OUT}=5A,L=6.8uH



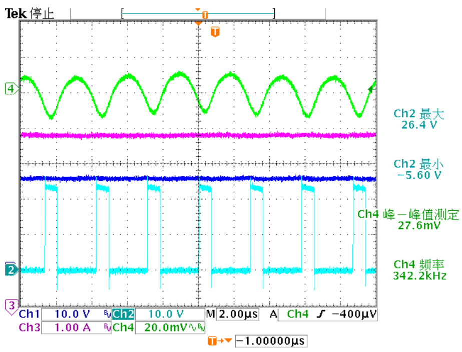
Output Ripple Voltage

V_{IN}=36V, V_{OUT}=5V, I_{OUT}=0A,L=6.8uH



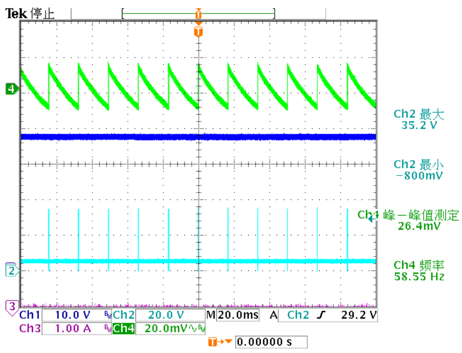
Output Ripple Voltage

V_{IN}=36V, V_{OUT}=5V, I_{OUT}=5A,L=6.8uH



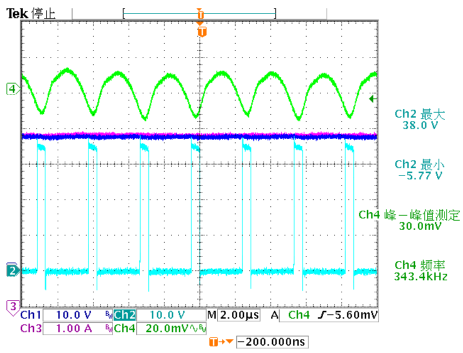
Loop Response

V_{IN}=12V, V_{OUT}=5V, L=6.8uH, I_{OUT}=1.25A-2.5A



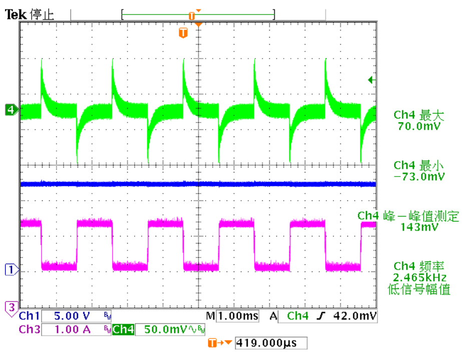
Loop Response

V_{IN}=12V, V_{OUT}=5V, L=6.8uH, I_{OUT}=2.5A-3.75A

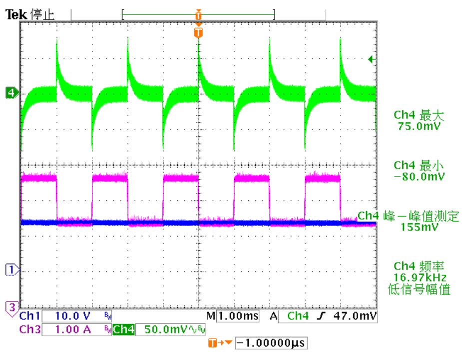


Loop Response

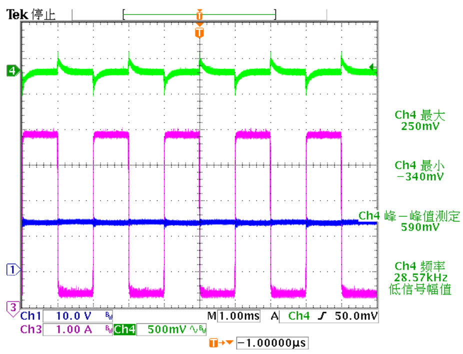
V_{IN}=12V, V_{OUT}=5V, L=6.8uH, I_{OUT}=0A-5A



Loop Response



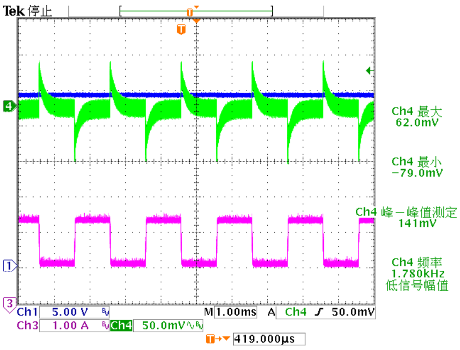
Loop Response



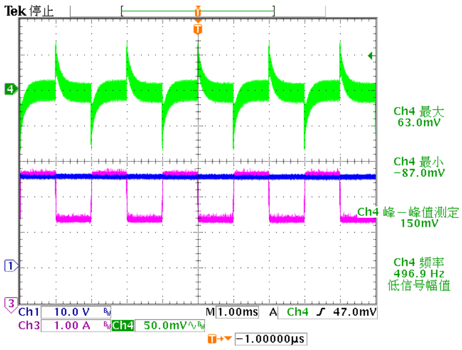
Loop Response

65V Input, 5A Output,
Asynchronous Step-Down DC/DC Converter

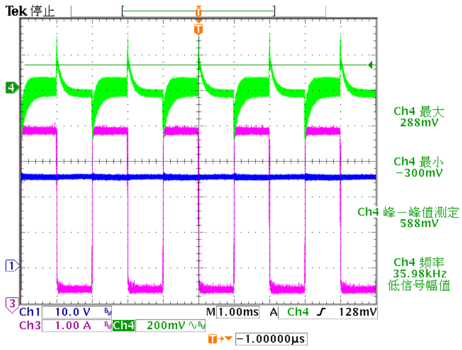
V_{IN}=24V, V_{OUT}=5V, L=6.8uH, I_{OUT}=1.25A-2.5A



V_{IN}=24V, V_{OUT}=5V, L=6.8uH, I_{OUT}=2.5A-3.75A

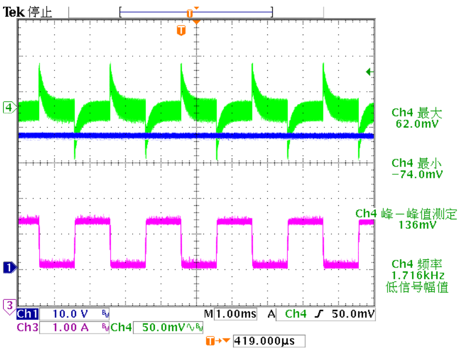


V_{IN}=24V, V_{OUT}=5V, L=6.8uH, I_{OUT}=0A-5A



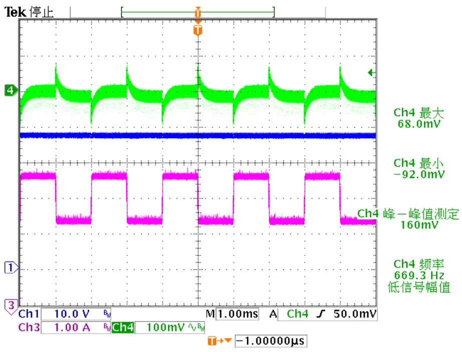
Loop Response

V_{IN}=36V, V_{OUT}=5V, L=6.8uH, I_{OUT}=1.25A-2.5A



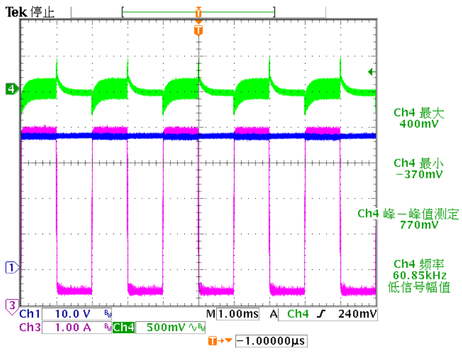
Loop Response

V_{IN}=36V, V_{OUT}=5V, L=6.8uH, I_{OUT}=2.5A-3.75A



Loop Response

V_{IN}=36V, V_{OUT}=5V, L=6.8uH, I_{OUT}=0A-5A



Functional Block Diagram

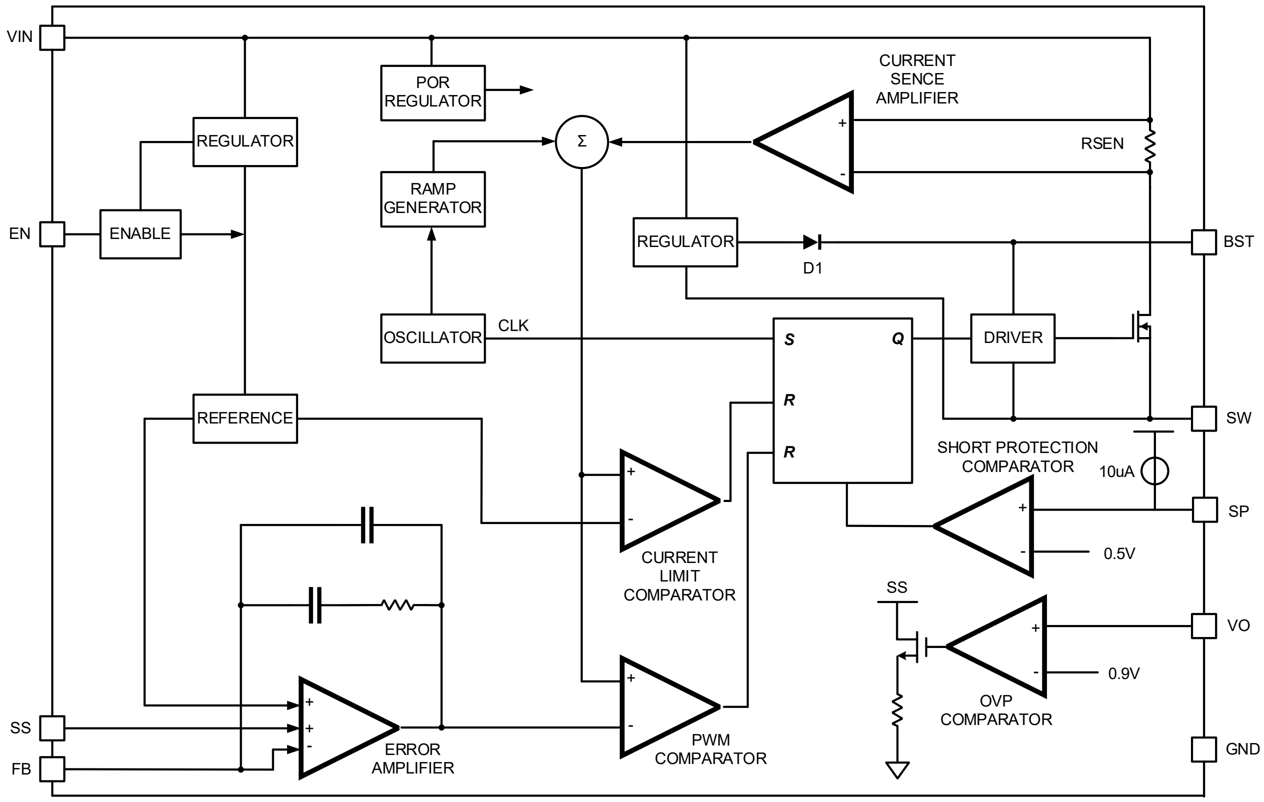


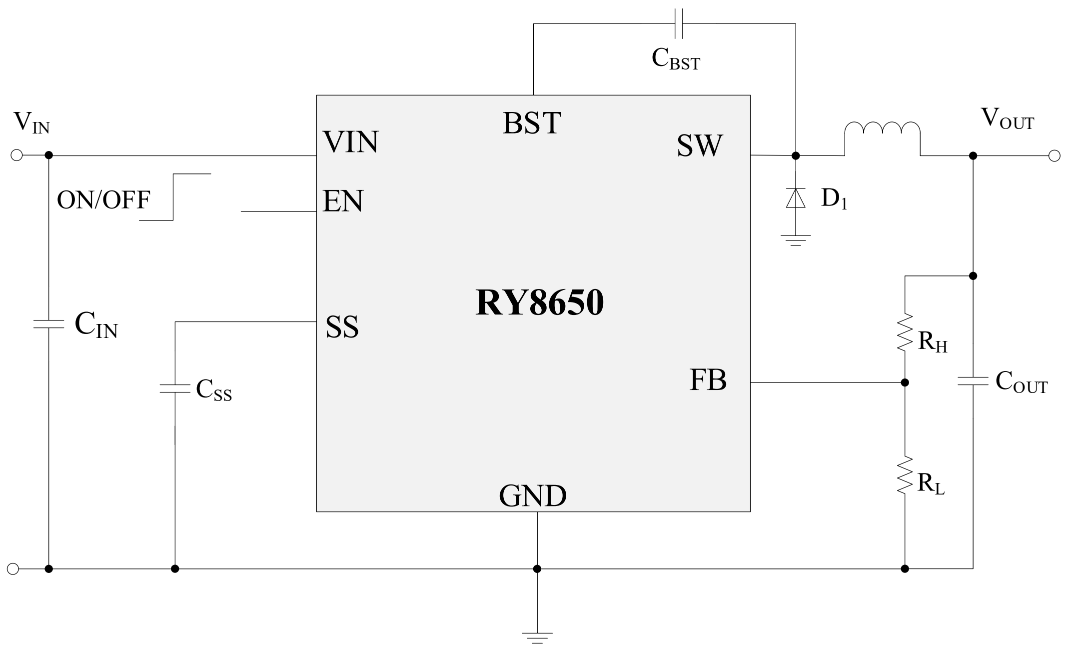
Figure 3. Functional Block Diagram

Functional Description

The RY8650 is an asynchronous, current-mode, step-down regulator. It achieves 5A of continuous output current from 4.8V to 65V input voltage.

Applications Information

Negative Output Voltage Set



Output Voltage Set

The output voltage is determined by the resistor divider connected at the FB pin, and the voltage ratio is:

$$V_{FB} = V_{OUT} \cdot \frac{R_H}{R_L + R_H}$$

Choose R_H and R_L to program the proper output voltage. To minimize the power consumption under light loads, it is desirable to choose large resistance values for both R_H and R_L. A value of between 10kΩ and 1MΩ is highly recommended for both resistors. If R_H =100kΩ is chosen, then RL can be calculated by the calculation formula as follows:

$$R_L = \frac{0.8V \times R_H}{(V_{OUT} - 0.8V)}$$

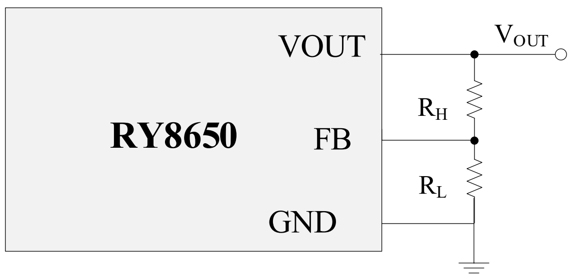


Figure 4. Output voltage setting

Input Capacitor C_{IN}

The purpose of the input capacitor is to stabilize the input voltage and provide the AC input current for the synchronous step-down DC/DC regulator. The RMS value of the input capacitor ripple current can be estimated using the following formula:

$$I_{CIN} = I_{OUT} * \sqrt{D * (1 - D)} = I_{OUT} * \sqrt{\frac{V_{OUT}}{V_{IN}} * (1 - \frac{V_{OUT}}{V_{IN}})}$$

Where I_{OUT} is the load current; V_{OUT} is the output voltage;; V_{IN} is the input voltage;
When the input ripple voltage is determined, the input capacitor can be selected by:

$$C_{IN} = \frac{I_{OUT}}{f_{sw} * \Delta V_{IN}} * D * (1 - D) = \frac{I_{OUT}}{f_{sw} * \Delta V_{IN}} * \frac{V_{OUT}}{V_{IN}} * (1 - \frac{V_{OUT}}{V_{IN}})$$

To minimize the potential noise problem, place 4.7uF*3/100V capacitors in typical application as close to the VIN and GND pins as possible.

Output Capacitor C_{OUT}

The output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor.
By choosing the appropriate output capacitor to meet the output voltage ripple, noise requirements. When selecting capacitors, both steady-state ripple and transient requirements must be considered, and the output ripple can be calculated by the following formula:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{sw} * L} * (1 - \frac{V_{OUT}}{V_{IN}}) * (R_{ESR} + \frac{1}{8 * f_{sw} * C_{OUT}})$$

where C_{OUT} is the output capacitor value; R_{ESR} is the equivalent series resistance value of the output capacitor.
For the best performance, it is recommended to use X7R or better grade ceramic capacitor with greater than 50µF capacitance. Place this ceramic capacitor really close to the VOUT and GND pins to minimize the loop area formed by C_{OUT}, and the VOUT/GND pins.

Inductor

The inductor is used to supply constant current to the output load, and the value determines the ripple current which affect the efficiency and the output voltage ripple. The ripple current is typically allowed to be 40% of the maximum switch current limit, thus the inductance value can be calculated by:

$$L = \frac{V_{OUT}}{f_{sw} * \Delta I_L} * (1 - \frac{V_{OUT}}{V_{IN}})$$

Where ΔI_L is the peak-to-peak inductor ripple current.

External Soft-start

The meaning of t_{ss} is the time for the output voltage to establish a range from 10% to 90%, as shown in the following figure 5:

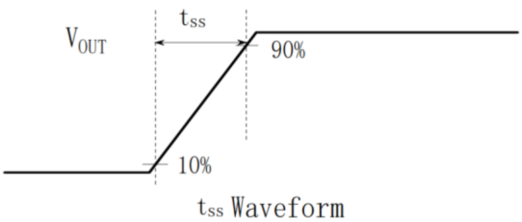


Figure 5. t_{ss} schematic diagram

The soft start time t_{ss} can be calculated by the following equation:

$$t_{ss} = \frac{C_{ss}(nF) * V_{REF} * 0.8}{I_{ss}(\mu A)}$$

where C_{ss} is the soft-start capacitance connected between SS pin and AGND pin, I_{ss} is the internal current source of 1.8μA （It is designed to charge the external soft-start capacitor (C_{ss}) and generates a soft-start voltage ramping up from 0V to 3V.）, the typical value of V_{REF} is 0.8V.

External Bootstrap Capacitor

N-Channel MOSFET switch is integrated in the RY8650 to convert the input voltage to the regulated output voltage. Since the top MOSFET needs a gate voltage greater than the input voltage, a boost capacitor connected between BST and SW pins is required to drive the gate of the top switch. The boost capacitor is charged by the internal 4.3V rail when SW is low.

Connect a 0.1uF capacitor between BST and SW pin to supply current for the top switch driver.

External Diode

The RY8650 is an asynchronous step-down regulator. It requires an external catch diode between the SW pin and GND. The selected diode must have a reverse voltage rating equal to or greater than VIN(max). The peak current rating of the diode must be greater than the maximum inductor current.

Schottky diodes are typically a good choice for the diode due to their low forward voltage. The lower the forward voltage of the diode, the higher the efficiency of the regulator. Typically, diodes with higher voltage and current ratings have higher forward voltages. The select forward voltage of Schottky Diode must be less than the restriction of forward voltage in Figure 6 at operating temperature range to avoid the IC malfunction.

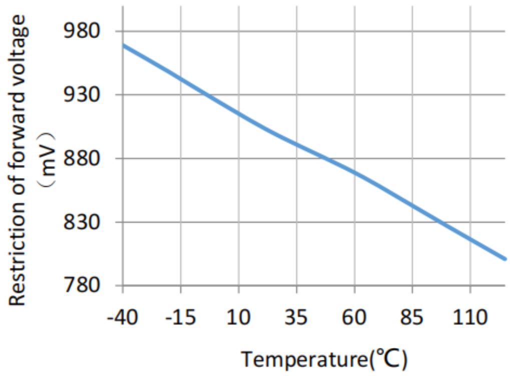


Figure6. Restriction of Forward Voltage vs Temperature

For the example design, the PDS760 Schottky diode is selected for its lower forward voltage and good thermal characteristics compared to smaller devices. The typical forward voltage of the PDS760 is 0.52 V at 5 A.

Maximum Switching Frequency and OCP method

The RY8650 utilizes peak current-mode control to regulate the output voltage.To protect the converter in overload conditions at higher switching frequencies and input voltages, the RY8650 implements a frequency fold-back.

The oscillator frequency is divided by 4 as the FB voltage drops from 0.8V to below 0.35V. When the FB voltage rise above 0.4V, the frequency exist fold-back state. The oscillator frequency is divided by 8 as the FB voltage drops to 0.18V. When the FB voltage rise above 0.2V, the frequency exist fold-back state.

When the output voltage is forced low by the shorted load, the inductor current decreases slowly during the switch off time. The frequency fold-back effectively increases the off time by increasing the period of the switching cycle providing more time for the inductor current to ramp down.

The chip adopts peak current control, and can't control the valley current in time. The frequency fold-back effectively increases the off time by increasing the period of the switching cycle providing more time for the inductor current to ramp down. With a maximum frequency fold-back ratio of 8, there is a maximum frequency at which the inductor current can be controlled by frequency fold-back protection.

The following equation calculates the maximum switching frequency at which the inductor current will remain under control when V_{OUT} is forced to V_{OUT_SC}. The selected operating frequency should not exceed the calculated value.

$$f_{sw\_sc} = \frac{f_{DIV}}{t_{ON}} \times (\frac{I_{LIM} \times R_{dc} + V_{OUT\_SC} + V_d}{V_{IN} - I_{LIM} \times R_{DS\_ON} + V_d})$$

where f_{DIV} means frequency divide equals (1,4,8), t_{ON} means controllable on time, I_{LIM} means current limit, R_{dc} means inductor resistance, V_{OUT_SC} means output voltage during short, V_d means diode voltage drop, R_{DS_ON} means switch on resistance.

The following equation calculates the maximum switching frequency limitation set by the minimum controllable on time and the input to output step down ratio. Setting the switching frequency above this value will cause the regulator to skip switching pulses to achieve the low duty cycle required to regulate the output at maximum input voltage.

$$f_{sw\_maxskip} = \frac{1}{t_{ON}} \times (\frac{I_O \times (R_{dc} + V_{OUT}) + V_d}{V_{IN} - I_O \times R_{DS\_ON} + V_d}$$

Where I_O means output current.

Thermal Shutdown Protection

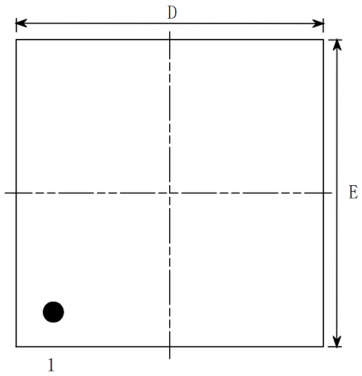
If the junction temperature of RY8650 is higher than the thermal shutdown temperature (typical 170°C), the IC will enter thermal shutdown protection mode. It will remain in this state until the junction temperature decreases below 150°C. After exiting this state, the IC auto retries to normal operation.

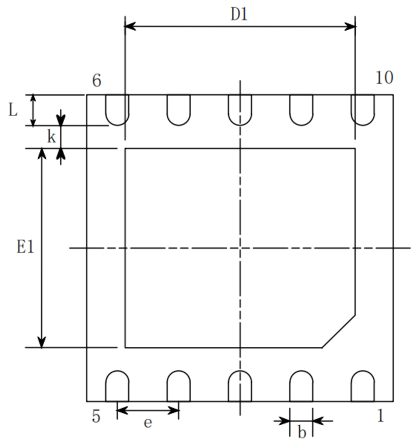
Layout Design

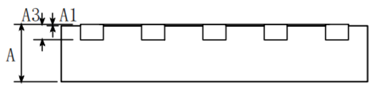
To achieve a higher efficiency and better noise immunity, following components should be placed close to the IC: C_{IN} and C_{OUT}.

1) C_{IN} must be close to the pins VIN and GND. The loop area formed by C_{IN} and GND must be minimized.
2) C_{OUT} must be close to the pins VOUT and GND. The loop area formed by C_{OUT} and GND must be minimized.
3) Place the FB components (R_H, R_L) as close to the FB pin as possible. Avoid routing the FB trace near SW as it is noise sensitive.
4) Make Vin, Vout and ground bus connections as wide as possible. This reduces any voltage drops on the input or output paths of the converter and maximizes efficiency.
5) It is desirable to maximize the PCB copper area connecting to the GND pin to achieve the best thermal and noise performance. If the board space allowed, a ground plane is highly desirable.

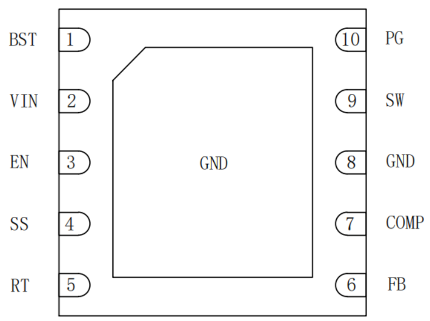
DFN4×4-10 Package Outline Drawing



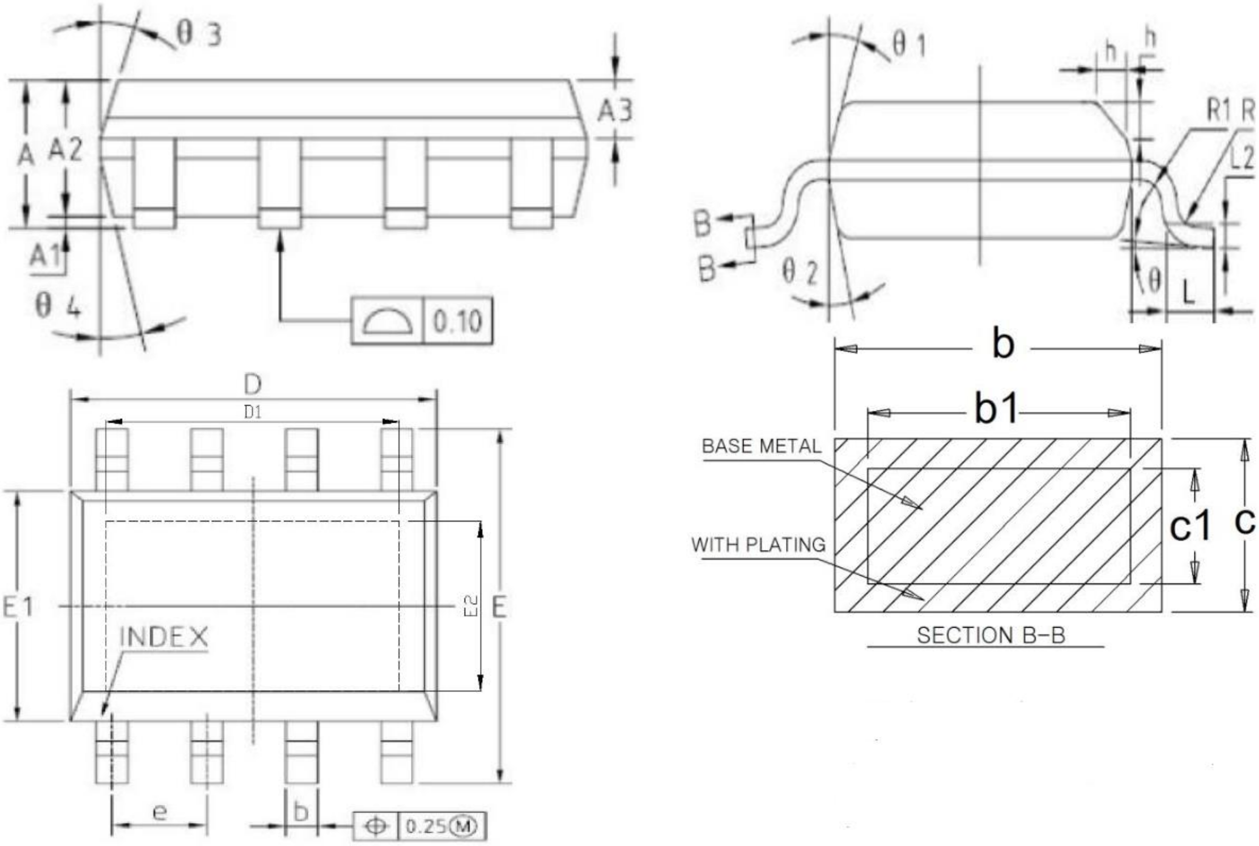




SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.203REF		
D	4.00BSC		
E	4.00BSC		
D1	2.90	3.00	3.10
E1	2.50	2.60	2.70
k	0.30REF		
b	0.25	0.30	0.35
e	0.80BSC		
L	0.30	0.40	0.50



ESOP8



SYMBOL	MIN	MON	MAX
A	1.45	1.55	1.65
A1	0.00	–	0.10
A2	1.353	1.40	1.453
A3	0.55	0.60	0.65
b	0.38	–	0.51
b1	0.37	0.42	0.47
c	0.17	–	0.25
c1	0.17	0.20	0.23
D	4.85	4.90	4.95
E	5.85	6.000	6.20
E1	3.85	3.90	3.95
D1	3.172REF		
E2	2.283REF		
e	1.245	1.27	1.295
L	0.45	0.65	0.85
L1	–	1.040REF	–
L2	–	0.250BSC	–

Modify Information

Version	Modifications	Date
V1.0.3	Add new package	2025.05.14
V1.0.4	Update ESOP8 package Description	2025.06.04
V1.0.5	Delete AD10 package	2025.06.09
V1.0.6	Update ESOP8(AP) package	2025.08.22