100V 2A Async Step-Down Converter

Features

- Wide input voltage Range: 4.5V~100V
- Adjustable Output Voltage from 0.8V to VIN
- Low $R_{DS(ON)}$ Switches 500mΩ
- 420kHz Fixed Switching Frequency or 170-470kHz Adjustable Switching Frequency
- Duty Cycle up to 98%
- Short Circuit Protection
- Over Current Protection
- Internal Soft Startup
- Thermal Shutdown Protection
- Available in ESOP8 Packages

Applications

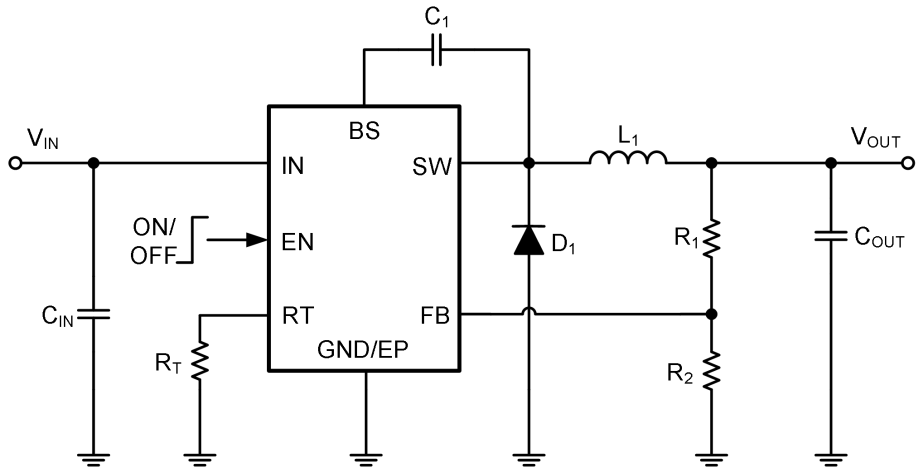
- LCD Monitor and LCD TV
- Battery-powered Equipment
- Entertainment Devices
- Digital Home Appliances: Digital TVs
- ADSL Modem Portable Instruments

General Description

The RY81020 is a monolithic IC designed for step-down DC/DC converters, featuring low EMI, the ability to drive 2A continuous current, and excellent load and line regulation. The RY81020 can also operate at 98% duty cycle for low dropout operation, and internal soft-start allows for low inrush currents, extending battery life in portable systems. In terms of protection features, it features cycle-by-cycle peak current limiting, short-circuit protection, thermal shutdown and undervoltage lockout.

The RY81020 is available in ESOP8 packages.

Typical Application Circuit

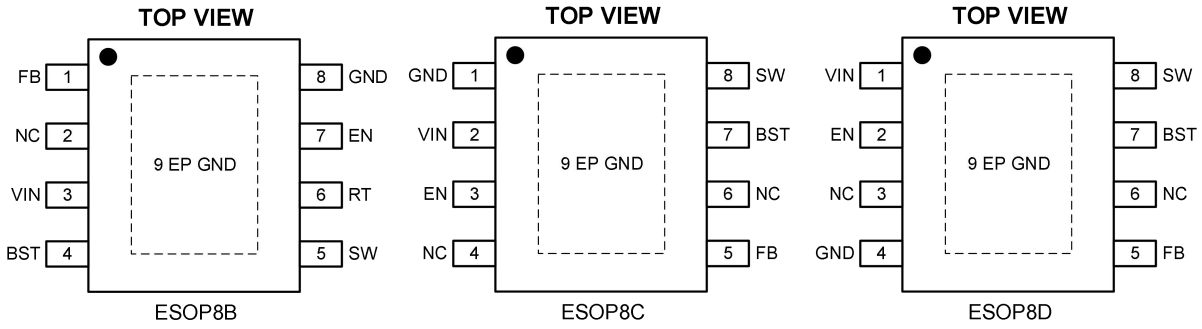


Basic Application Circuit

100V 2A Async Step-Down Converter

Pin Description

Pin Configuration



Pin Description

Pin No.			Name	Function
ESOP8B	ESOP8C	ESOP8D		
1	5	5	FB	Feedback input of voltage regulation comparator.
2	4, 6	3, 6	NC	No connection.
3	2	1	VIN	Power Supply Pin.
4	7	7	BST	Bootstrap. A capacitor connected between SW and BS pins is required to form a floating supply across the high-side switch driver.
5	8	8	SW	Switching Pin.
6	-	-	RT	Frequency Selection. Connect an external resistor from the RT pin to ground to set the switching frequency.
7	3	2	EN	Drive this pin to a logic-high to enable the IC. Drive to a logic-low to disable the IC and enter micro-power shutdown mode.
8	1	4	GND	Ground Pin.
EP	EP	EP	EPAD	Exposed pad of the package. No internal electrical connection. Solder the EP to the GND pin and connect to a large copper plane to reduce thermal resistance.

Order Information (1)

Marking	Part No.	Model	Description	Package	T/R Qty
LIYLL	70301814	RY81020BP8	RY81020BP8 Async Buck, 4.5V-100V, 2A, 170-470kHz, VFB 0.8V, ESOP8B	ESOP8B	4000PCS
LJYLL	70301815	RY81020CP8	RY81020CP8 Async Buck, 4.5V-100V, 2A, 420kHz, VFB 0.8V, ESOP8C	ESOP8C	4000PCS

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LKYLL	70301816	RY81020DP8	RY81020DP8 Async Buck, 4.5V-100V, 2A, 420kHz, VFB 0.8V, ESOP8D	ESOP8D	4000PCS

Note (1): All RYCHIP parts are Pb-Free and adhere to the RoHS directive.

Specifications

Absolute Maximum Ratings (1) (2)

Item	Min	Max	Unit
VIN voltage	-0.3	110	V
EN voltage	-0.3	110	V
FB voltage	-0.3	6.5	V
SW voltage	-0.5	110	V
BS to SW voltage	-0.3	5	V
Operating junction temperature, T_J	-40	150	°C
Storage temperature, T_{stg}	-65	150	°C

Note (1): Exceeding these ratings may damage the device.

Note (2): The device is not guaranteed to function outside of its operating conditions.

ESD Ratings

Item	Description	Value	Unit
$V_{(ESD-HBM)}$	Human Body Model (HBM) ANSI/ESDA/JEDEC JS-001-2014 Classification, Class: 2	±2000	V
$V_{(ESD-CDM)}$	Charged Device Mode (CDM) ANSI/ESDA/JEDEC JS-002-2014 Classification, Class: C0b	±200	V
$I_{LATCH-UP}$	JEDEC STANDARD NO.78E APRIL 2016 Temperature Classification, Class: I	±150	mA

Recommended Operating Conditions

Item		Min	Max	Unit
Operating junction temperature (1)		-40	125	°C
Operating temperature		-40	85	°C
Input voltage V_{IN}		4.5	100	V
Output voltage V_{OUT}		0.8	30	V
Output Current	I_{OUT}	0	2	A
	$I_{OUT(PEAK)}$<100ms	0	2.5	A

Note (1): All limits specified at room temperature (T_A = 25°C) unless otherwise specified. All room temperature limits are 100% production tested. All limits at temperature extremes are ensured through correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).

Thermal Information

Item	Description	Value	Unit
$R_{\theta JA}$	Junction-to-ambient thermal resistance (1)(2)	48.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	52.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	25.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	8.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	25.2	°C/W
$R_{\theta JCbot}$	Junction-to-case(bottom) thermal resistance	6.5	°C/W

Note (1): The package thermal impedance is calculated in accordance to JESD 51-7.

Note (2): Thermal Resistances were simulated on a 4-layer, JEDEC board.

Electrical Characteristics (1) (2)

V_{IN}=48V, T_A=25°C, unless otherwise specified.

Parameter	Symbol	Test Conditions	Min	Typ.	Max	Unit
Input Voltage Range	V_{IN}		4.5		100	V
Quiescent Current	I_Q	EN = 5V		175	300	μA
Shutdown Current	I_{SD}	EN = GND			3	μA
Feedback Voltage	V_{FB}		784	800	816	mV
Under-voltage Lockout	V_{UVLO}			4.0		V
Under-voltage Lockout Hysteresis	V_{UVLO_HYS}			295		mV
EN Rising Threshold	V_{ENH}		1.5			V
EN Falling Threshold	V_{ENL}				0.4	V
EN Threshold Hysteresis	V_{EN_HYS}			200		mV
High-side FET on Resistance	$R_{DS(ON)\_H}$	I_{SW} = 1000mA		500		mΩ
High side FET Current Limit	I_{LIM_H}	FB = 90%			3	A
Adjustable Switching Frequency	F_{SWA}		170		470	kHz
Fixed Switching Frequency	F_{SW}			420		kHz
Soft Start	t_{SS}		1	2	3	ms
Thermal Shutdown Temperature	T_{SD}			170		°C
Thermal Shutdown Hysteresis	T_{SD_HYS}			30		°C

Note (1): MOSFET on-resistance specifications are guaranteed by correlation to wafer level measurements.

Note (2): Thermal shutdown specifications are guaranteed by correlation to the design and characteristics analysis.

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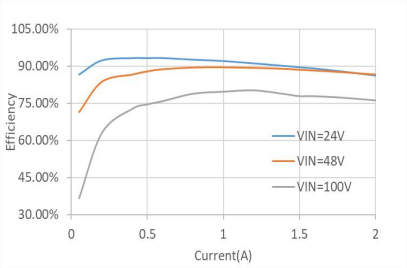
Typical Performance Characteristics (1) (2)

Note (1): Performance waveforms are tested on the evaluation board.

Note (2): V_{IN} =48V, T_A = +25ºC, PFM mode in light load, unless otherwise noted.

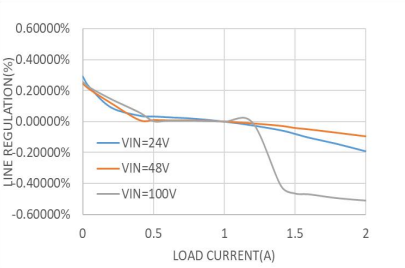
Efficiency vs. Load Current

V_{OUT}=12.0V



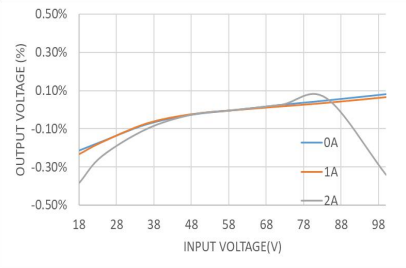
Load Regulation

V_{OUT}=12.0V



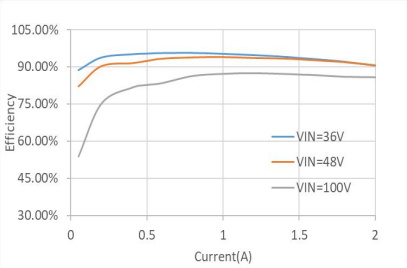
Line Regulation

V_{OUT}=12.0V



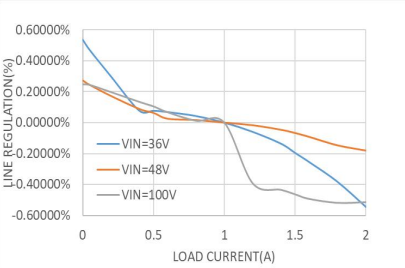
Efficiency vs. Load Current

V_{OUT}=24.0V



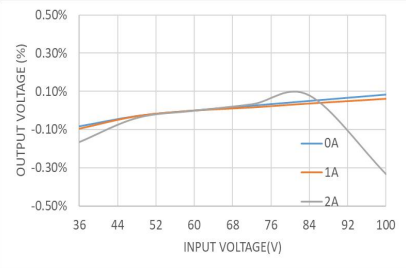
Load Regulation

V_{OUT}=24.0V



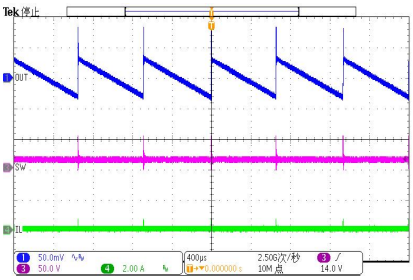
Line Regulation

V_{OUT}=24.0V



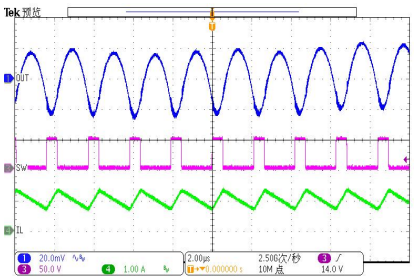
Output Ripple Voltage

V_{OUT}=12.0V, I_{OUT}=0A



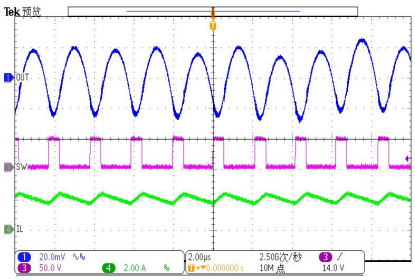
Output Ripple Voltage

V_{OUT}=12.0V, I_{OUT}=1A



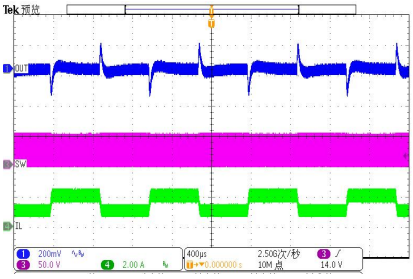
Output Ripple Voltage

V_{OUT}=12.0V, I_{OUT}=2A



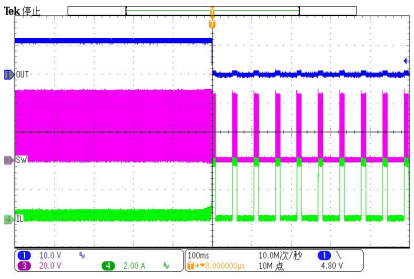
Loop Response

V_{OUT}=12.0V, I_{OUT}=1A-2A



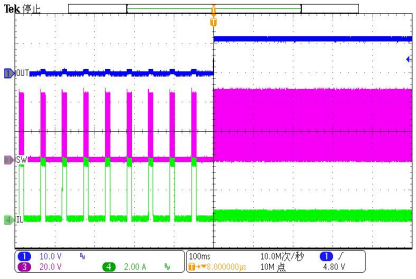
Short Circuit Entry

V_{OUT}=12.0V



Short Circuit Recovery

V_{OUT}=12.0V



Enable Startup at No Load

V_{OUT}=12.0V, I_{OUT}=0A

Enable Shutdown at No Load

V_{OUT}=12.0V, I_{OUT}=0A

Enable Startup at Full Load

V_{OUT}=12.0V, I_{OUT}=2A (RLoad=6Ω)

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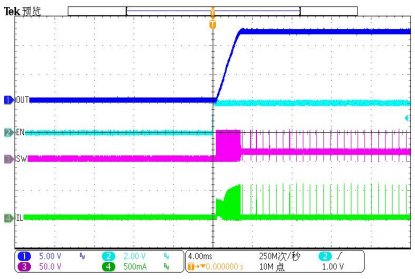
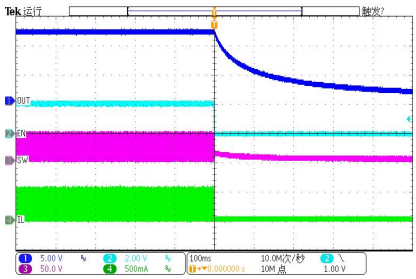
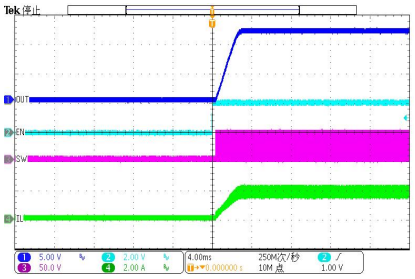
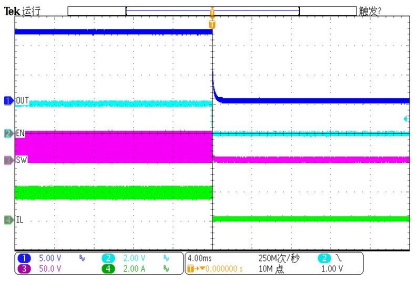
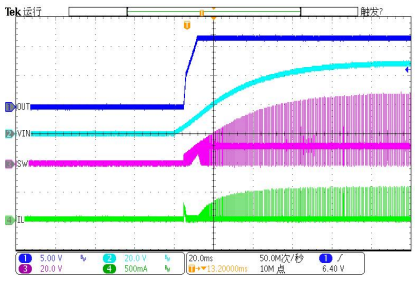
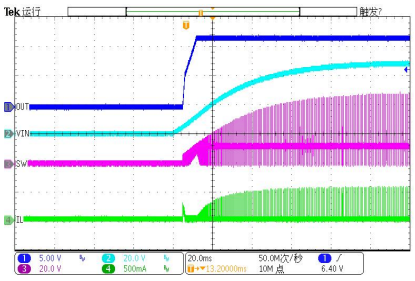
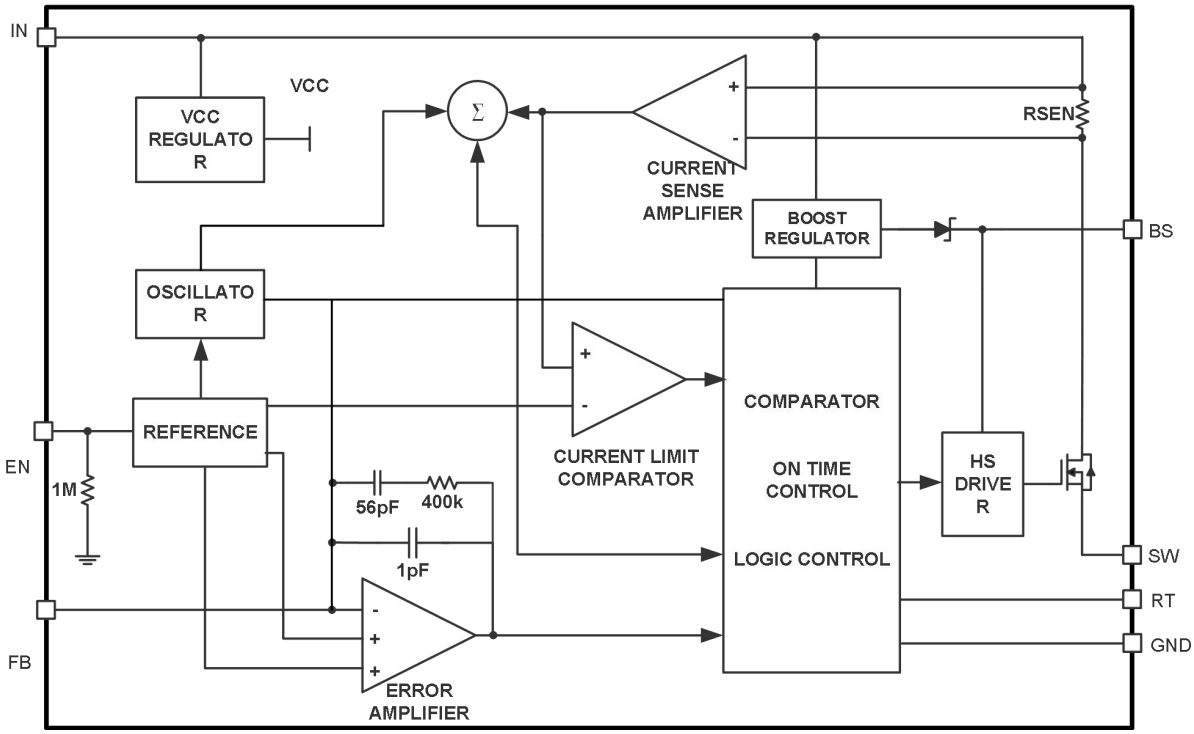
		
Enable Shutdown at Full Load	**Power Up at No Load**	**Power Up at Full Load**
V_{OUT}=12V, I_{OUT}=2A (RLoad=6Ω)	V_{OUT}=12.0V, I_{OUT}=0A	V_{OUT}=12V, I_{OUT}=2A (RLoad=6Ω)
		

100V 2A Async Step-Down Converter

Functional Block Diagram



Block Diagram

Functions Description

General Description

The RY81020 DC/DC converter provides up to 2A of output from a 4.5V to 100V input voltage source. The RY81020 is a high output current monolithic switch-mode step-down DC-DC converter. The RY81020BP8 operates at a fixed 420kHz switching frequency, the RY81021CP8 operates at an adjustable switching frequency from 170kHz to 470kHz and features a slope-compensated current-mode architecture. The external shutdown function can be controlled by a logic level followed by a standby mode. In terms of protection features, thermal shutdown is used to prevent damage from over-temperature operation, and current limit is used to prevent the output switches from over-current operation. When the current limit function occurs, the switching frequency will be reduced if V_{FB} is below 0.8V.

Internal Soft Start

The RY81020 employs an internal soft-start control ramp that allows the output voltage to gradually reach a steady-state operating point, thereby reducing start-up stresses and current surges. The soft-start feature produces a controlled, monotonic output voltage start-up. The soft-start time is internally set to 1.8ms.

Startup and Shutdown

If both VIN and EN are higher than the appropriate thresholds, the chip starts. The reference block starts first, generates stable reference voltage and currents, and then the internal regulator is enabled. The regulator provides stable supply for the remaining circuitries. Three events can shut down the chip: EN low, VIN low and thermal shutdown. In the shutdown procedure, the signaling path is first blocked to avoid any fault triggering. The comp

voltage and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command.

Under-voltage Lockout (UVLO)

Under-voltage lockout (UVLO) is used to protect the chip when the supply voltage is insufficient. The rising threshold of UVLO is about 4.0V, while the falling threshold is always 3.705V.

Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die temperature exceeds 150°C, it shuts down the whole chip. When the temperature falls below its lower threshold (Typ. 130°C) the chip is enabled again.

Applications Information

Typical Application

The feedback voltage at FB is compared to an internal 0.8V reference. The RY81020 voltage regulation loop regulates the output voltage by maintaining the FB voltage equal to the internal reference voltage, V_{FB}. A resistor divider programs the ratio from output voltage V_{OUT} to FB. For a target V_{OUT} setpoint, calculate R_2 based on the selected R_1 using.

$$V_{OUT} = 0.8V \times \frac{R1 + R2}{R2}$$

recommends selecting R_1 in the range of 100kΩ to 1MΩ for most applications. A larger R_1 consumes less DC current, which is mandatory if light-load efficiency is critical. R_1 larger than 1MΩ is not recommended as the feedback path becomes more susceptible to noise. It is important to route the feedback trace away from the noisy area of the PCB and keep the feedback resistors close to the FB pin.

V_{OUT}(V)	R1(KΩ)	R2(KΩ)	L1(μH)	C1(nF)	C_{IN}(μF)	C_{OUT}(μF)	C_{FF}(pF) Opt.
1.2	5	10	10	100	4.7	22×2	C_{FF} Chapter
1.5	8.75	10	10	100	4.7	22×2	C_{FF} Chapter
1.8	12.5	10	15	100	4.7	22×2	C_{FF} Chapter
2.5	21.25	10	15	100	4.7	22×2	C_{FF} Chapter
3.3	31.25	10	22	100	4.7	22×2	C_{FF} Chapter
5.0	52.5	10	33	100	4.7	22×2	C_{FF} Chapter
12	140	10	33	100	4.7	22×2	C_{FF} Chapter
24	290	10	68	100	4.7	22×2	C_{FF} Chapter

However, if there is loop instability in the application, try the following recommended values：

V_{OUT}(V)	R1(KΩ)	R2(KΩ)	L1(μH)	C1(nF)	C_{IN}(μF)	C_{OUT}(μF)	C_{FF}(pF) Opt.
1.2	0.5	1	10	100	4.7	22×2	51pF
1.5	0.875	1	10	100	4.7	22×2	51pF
1.8	1.25	1	15	100	4.7	22×2	51pF
2.5	2.125	1	15	100	4.7	22×2	51pF
3.3	3.125	1	22	100	4.7	22×2	51pF
5.0	5.25	1	33	100	4.7	22×2	51pF
12	14	1	33	100	4.7	22×2	51pF

24	29	1	68	100	4.7	22×2	51pF

All the external components are the suggested values, the final values are based on the application testing results.

Selecting the Inductor

The recommended inductor values are shown in the Application Diagram. It is important to guarantee the inductor core does not saturate during any foreseeable operational situation. The inductor should be rated to handle the maximum inductor peak current: Care should be taken when reviewing the different saturation current ratings that are specified by different manufacturers. Saturation current ratings are typically specified at 25°C, so ratings at maximum ambient temperature of the application should be requested from the manufacturer. The inductor value can be calculated with:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times F_{OSC}}$$

Where ΔI_L is the inductor ripple current. Choose inductor ripple current to be approximately 30% to 40% of the maximum load current. The maximum inductor peak current can be estimated as:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

Under light load conditions below 100mA, larger inductance is recommended for improved efficiency. Larger inductances lead to smaller ripple currents and voltages, but they also have larger physical dimensions, lower saturation currents and higher linear impedance. Therefore, the choice of inductance should be compromised according to the specific application.

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous and therefore requires a capacitor to supply AC current to the step-down converter while maintaining the DC input voltage. For a better performance, use ceramic capacitors placed as close to VIN as possible and a 0.1μF input capacitor to filter out high frequency interference is recommended. Capacitors with X5R and X7R ceramic dielectrics are recommended because they are stable with temperature fluctuations.

The capacitors must also have a ripple current rating greater than the maximum input ripple current of the converter. The input ripple current can be estimated with Equation:

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

From the above equation, it can be concluded that the input ripple current reaches its maximum at $V_{IN}=2V_{OUT}$ where $I_{CIN} = \frac{I_{OUT}}{2}$. For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitance value determines the input voltage ripple of the converter. If there is an input voltage ripple requirement in the system, choose the input capacitor that meets the specification. The input voltage ripple can be estimate with Equation:

$$\Delta V_{IN} = \frac{I_{OUT}}{F_{OSC} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Similarly, when V_{IN}=2V_{OUT}, input voltage ripple reaches its maximum of $\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{F_{OSC} \times C_{IN}}$.

Selecting the Output Capacitor

An output capacitor is required to maintain the DC output voltage. The output voltage ripple can be estimated with Equation:

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{OSC} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times F_{OSC} \times C_{OUT}}\right)$$

There are some differences between different types of capacitors. In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly caused by the capacitance. For simplification, the output voltage ripple can be estimated with Equation:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times {F_{OSC}}^2 \times L \times C_{OUT}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

A larger output capacitor can achieve a better load transient response, but the maximum output capacitor limitation should also be considered in the design application. If the output capacitor value is too high, the output voltage will not be able to reach the design value during the soft-start time and will fail to regulate. The maximum output capacitor value (C_{OUT_MAX}) can be limited approximately with Equation:

$$C_{OUT\_MAX} = \left(I_{LIM\_AVG} - I_{OUT}\right) \times T_{SS} / V_{OUT}$$

Where L_{LIM_AVG} is the average start-up current during the soft-start period, and T_{SS} is the soft- start time.

On the other hand, special attention should be paid when selecting these components. The DC bias of these capacitors can result in a capacitance value that falls below the minimum value given in the recommended capacitor specifications table.

The ceramic capacitor's actual capacitance can vary with temperature. The capacitor type X7R, which operates over a temperature range of −55°C to +125°C, will only vary the capacitance to within ±15%. The capacitor type X5R has a similar tolerance over a reduced temperature range of −55°C to +85°C. Many large value ceramic capacitors, larger than 1uF are manufactured with Z5U or Y5V temperature characteristics. Their capacitance can drop by more than 50% as the temperature varies from 25°C to 85°C. Therefore, X5R or X7R is recommended over Z5U and Y5V in applications where the ambient temperature will change significantly above or below 25°C.

External Bootstrap Diode

Add an external bootstrap diode when the system has a fixed 5V input or when the power supply generates a 5V output. This helps improve the efficiency of the regulator. The bootstrap diode can be a low-cost one. This diode is also recommended for high-duty– cycle operation (when $\frac{V_{OUT}}{V_{IN}} > 65\%$) and high output voltage (V_{OUT}>12V) applications.

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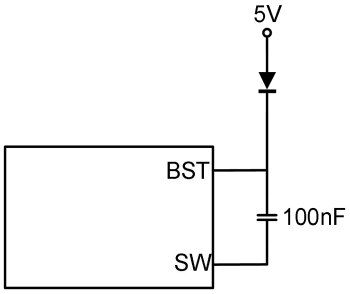


External Bootstrap Diode

PC Board Layout Consideration

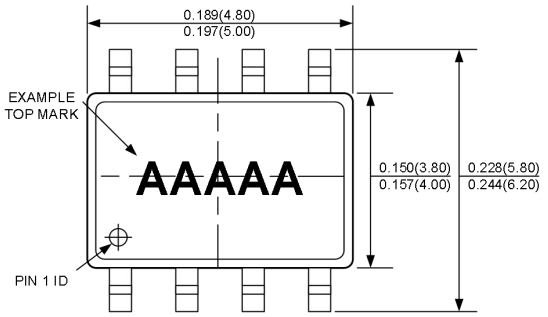
Efficient PCB layout is critical for stable operation. For best results, follow the guidelines below.

1. V_{IN} and GND traces should be as wide as possible to reduce trace impedance. The wide areas are also of advantage from the viewpoint of heat dissipation.
2. The input capacitor and output capacitor should be placed as close to the device as possible to minimize trace impedance.
3. Provide sufficient vias for the input capacitor and output capacitor.
4. Keep the SW trace as physically short and wide as practical to minimize radiated emissions.
5. Do not allow switching current to flow under the device.
6. A separate V_{OUT} path should be connected to the upper feedback resistor.
7. Make a Kelvin connection to the GND pin for the feedback path.
7. Voltage feedback loop should be placed away from the high-voltage switching trace, and preferably has ground shield.
9. The trace of the V_{FB} node should be as small as possible to avoid noise coupling.
10. The GND trace between the output capacitor and the GND pin should be as wide as possible to minimize its trace impedance.

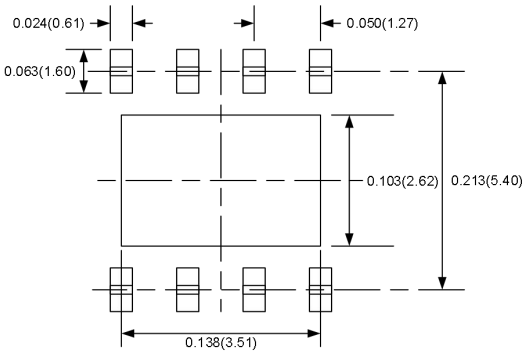
100V 2A Async Step-Down Converter

Package Description

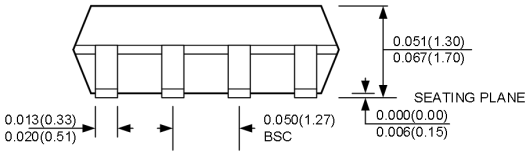
ESOP8 (EXPOSED PAD)



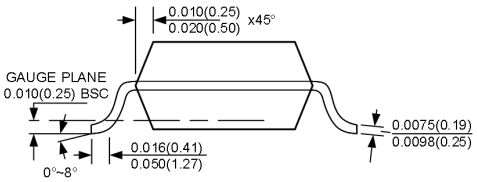
TOP VIEW



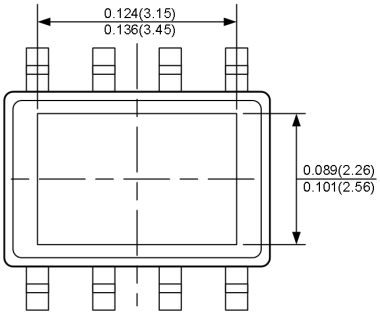
RECOMMENDED PAD LAYOUT



FRONT VIEW



SIDE VIEW



BOTTOM VIEW

NOTE:
1. CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2. PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3. PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5. DRAWING CONFORMS TO JEDEC MS-012, VARIATION BA.
6. DRAWING IS NOT TO SCALE.

修改信息

版本	修改内容	日期
V1.0.3	修改最小包装 3K-4K	2025.03.05