NSD11416-Q1

1CH, 160mΩ, 40V, Fully Protected Automotive Low-side Switch

Preliminary specifications subject to change without notice Datasheet (EN) 0V3

Product Overview

NSD11416-Q1 is a 160mΩ low-side switch with 48V clamp voltage for automotive applications. It's designed for driving resistive or inductive loads with one side connected to the battery. Internal 48V clamp circuit protects device from surge energy when fast demagnetization at turn-off.

With internal output current limitation, the device is protected in overload condition. Built-in thermal shutdown protects the chip from over-temperature and short-circuit. A thermal swing mechanism is built to limit dissipated power to decelerate power accumulation. Thermal shutdown, with automatic restart, allows the devices to recover normal operation as soon as a fault condition disappears.

An internal diagnose function is built to indicate any faults when thermal shutdown and open-drain conditions through an open-drain status output pin. This device operates in ambient temperatures from –40°C to 125°C.

Key Features

- AEC-Q100 qualified
- Drain current limitation: 2.5A
- 48V overvoltage clamp
- Thermal shutdown protection
- Thermal swing protection
- Fault diagnostic block
  - Thermal shutdown diagnosis
  - Open-drain diagnosis
- Very low standby current
- Very low electromagnetic susceptibility
- ESD protection

Applications

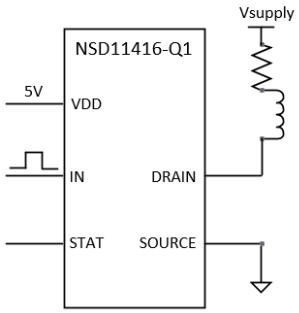
- Automotive Relays
- Solenoids
- Valves
- Lighting

Device Information

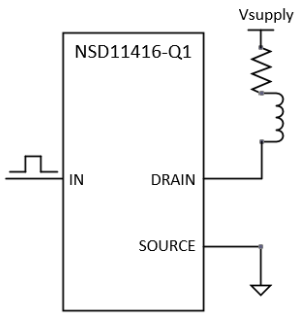
Part Number	*Package*	*Body Size*
NSD11416-Q1	SO-8	4.9mm x 3.9mm
	SOT223	6.48mm x 3.38mm

Typical Application

SO-8 package



SOT223 package



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1. Pin Configuration and Functions

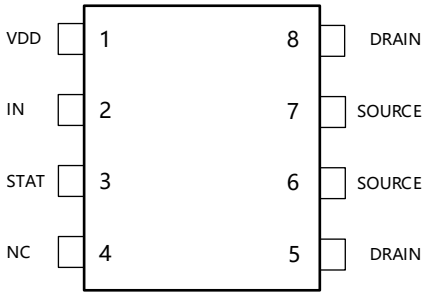


Table 1 SO-8 Pin Configuration and Description

PIN NO.	SYMBOL	FUNCTION
1	VDD	Power supply pin.
2	IN	CMOS compatible, voltage controlled input pin.
3	STAT	Open drain digital diagnostic pin.
4	NC	Not connect.
5, 8	DRAIN	PowerMOS drain.
6, 7	SOURCE	PowerMOS source.

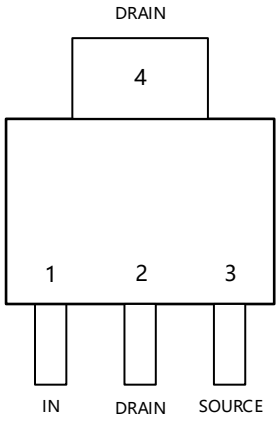


Table 2 SOT223 Pin Configuration and Description

PIN NO.	SYMBOL	FUNCTION
1	IN	CMOS compatible, voltage controlled input pin.
2, 4	DRAIN	PowerMOS drain.
3	SOURCE	PowerMOS source.

2. Block diagram

Figure 1. NSD11416-QSPR(SO-8) block diagram

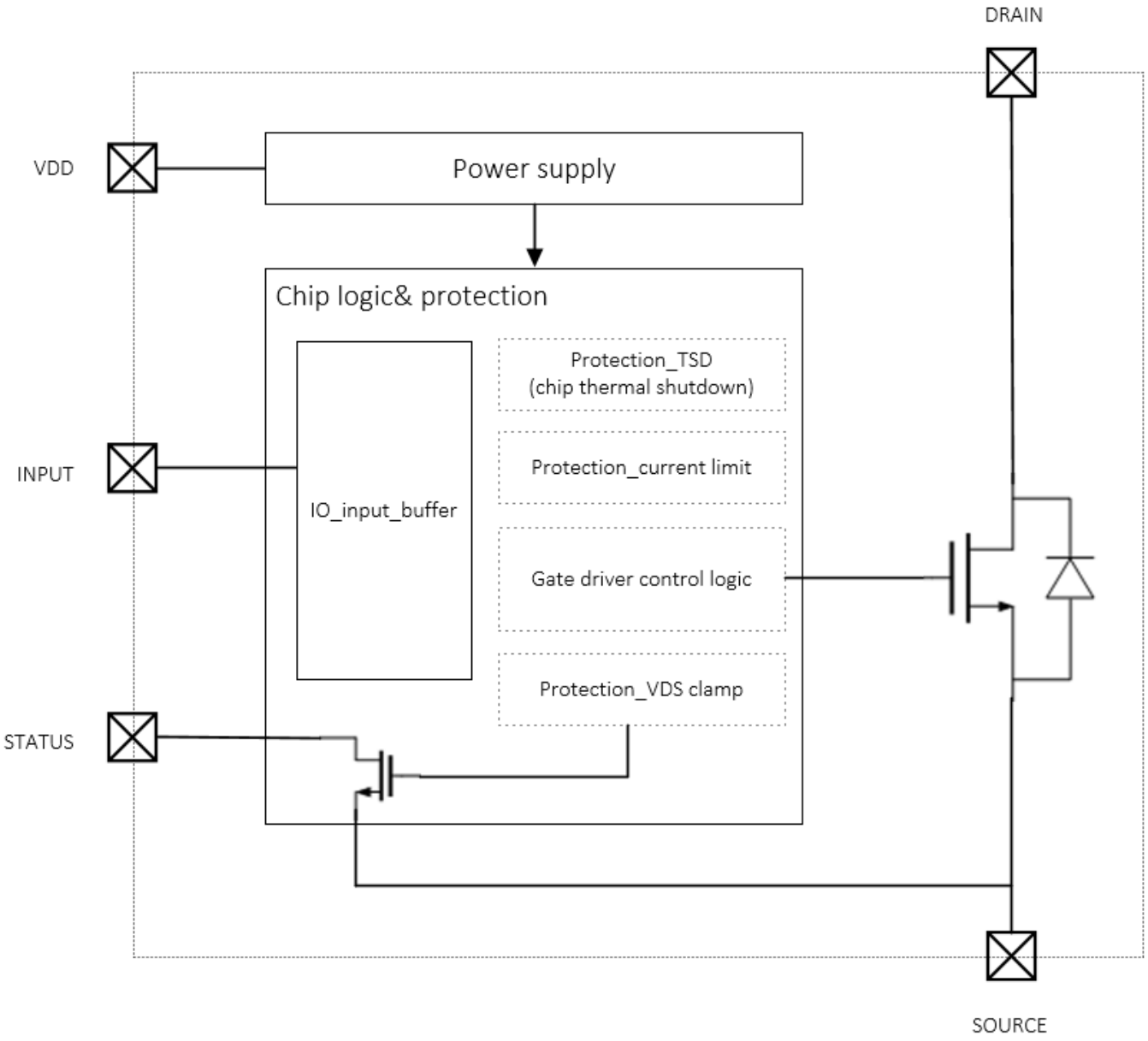
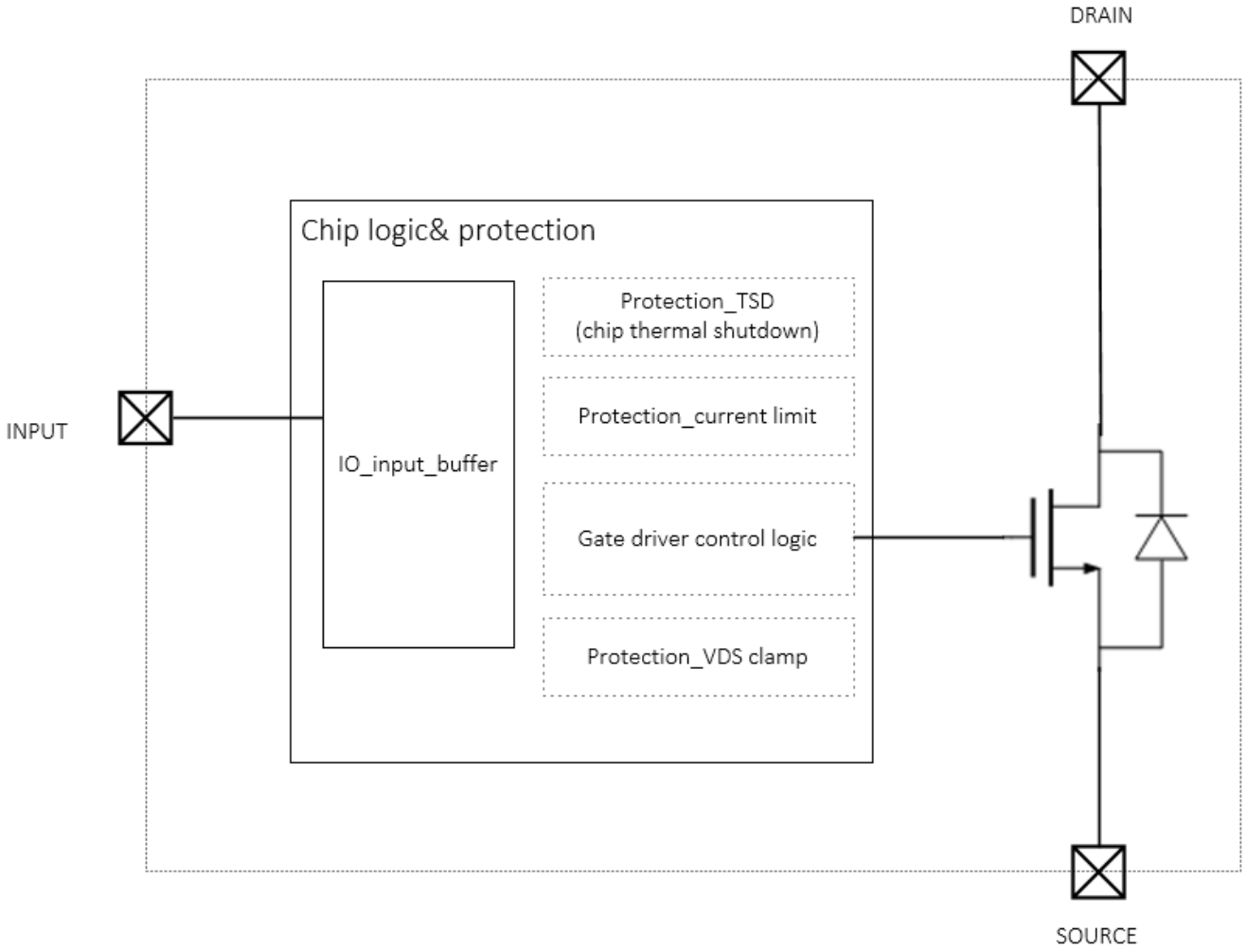


Figure 2. NSD11416-QSTBR(SOT223) block diagram



3. Absolute Maximum Ratings

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*
Drain-to-Source Voltage	V_{DS}			Internally clamped	V
DC Drain Current	I_D			Thermal limited	A
Reverse DC drain current	$-I_D$			4	A
VDD Pin Current	I_{VDD}	-1		10	mA
INPUT Pin Current	I_{IN}	-1		10	mA
STATUS Pin Current	I_{STAT}	-1		10	mA
Junction Temperature	T_J	-40		150	°C

Parameters	Symbol	Min	Typ	Max	Unit
Storage Temperature	T_{stg}	-55		150	°C
Electrostatic discharge, Human-body model	HBM	-4000		4000	V
Electrostatic discharge, Charged-device model	CDM	-750		750	V

4. Thermal Information

Parameters	Symbol	SO-8	SOT223	Unit
IC Junction-to-ambient Thermal Resistance	θ_{JA}	99	145	°C/W

5. Specifications

5.1. Electrical Characteristics

(VDD = VIN= 4.5 V to 5.5 V, Tj=-40°C to 150°C. Unless otherwise noted.)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power MOSFET						
Operating supply voltage	V_S	3.5	5	5.5	V	
ON-state resistance	R_{ON}			160	mΩ	ID = 1 A; Tj = 25°C; VDD = VIN = 5 V
				320	mΩ	ID = 1 A; Tj = 150°C; VDD = VIN = 5 V
Drain-source clamp voltage	V_{CLAMP}	46	48	56	V	V_{IN} = 0V, I_D = 1 A
Drain-source clamp threshold voltage	V_{CLTH}	40			V	V_{IN} = 0V, I_D = 2 mA
OFF-state output current	I_{DSS}	0		3	μA	VIN = 0 V; VDS = 13 V; Tj = 25°C
		0		5	μA	VIN = 0 V; VDS = 13 V; Tj = 125°C
Bode diode forward voltage	V_{BD}		0.8		V	ID = 1A; VIN = 0 V
Input section (SOT223 package only)						
Supply current from input pin	I_{ISS}		30	65	uA	ON-state: VDD = VIN = 5 V; VDS = 0 V
Input clamp voltage	V_{ICL}	5.5		7	V	IS = 1 mA
			-0.7			IS =-1 mA
Input threshold voltage	V_{INTH}	1		3.5	V	VDS = VIN; ID = 1 mA

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
VDD (SO8 pacakge only)						
Operating supply current	I_S		10	25	µA	OFF-state; Tj = 25°C; VIN = VDS = 0 V;
			25	65	µA	ON-state; VIN = 5 V; VDS = 0 V
Supply clamp voltage	V_{SCL}	5.5		7	V	ISCL = 1 mA
			-0.7			ISCL = -1 mA
Logic Input (SO8 package only)						
Low-level input voltage	V_{IL}			0.9	V	
Low-level input current	I_{IL}	1			µA	VIN = 0.9V
High-level input voltage	V_{IH}	2.1			V	
High-level input current	I_{IH}			10	µA	VIN = 2.1V
Input hysteresis voltage	$V_{I(hyst)}$	0.13			V	
Input clamp voltage	V_{ICL}	5.5		7		IIN = 1 mA
			-0.7			IIN = -1 mA
Status indicator (SO8 package only)						
Status low output voltage	V_{STAT}			0.5	V	I_{STAT} = 1 mA
Status leakage current	I_{LSTAT}			10	µA	V_{STAT} = 5 V
Status pin input capacitance	C_{STAT}			100	pF	V_{STAT} = 5 V
Status clamp voltage	V_{STCT}	5.5		7	V	I_{STAT} = 1 mA
			-0.7			I_{STAT} = - 1 mA
Open load detection (SO8 package only)						
Open load OFF-state voltage detection threshold	V_{OL}	1.1	1.2	1.3	V	VIN = 0 V
Delay between INPUT falling edge and STATUS falling edge in open load condition	$t_{d(STAT)}$		225		µs	IOUT = 0 A
Switching characteristics (Vsupply = VIN = 3.5V to 5.5 V, See Figure 6 for Switching timing characteristics)						
Turn-on delay time	$t_{d(ON)}$		8		µs	RL = 13 Ω, VCC = 13 V
Turn-off delay time	$t_{d(OFF)}$		18		µs	RL = 13 Ω, VCC = 13 V
Rise time	t_r		3		µs	RL = 13 Ω, VCC = 13 V

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Fall time	t_f		3		µs	RL = 13 Ω, VCC = 13 V
Switching energy losses at turn-on	W_{ON}		TBD		uJ	RL = 13 Ω, VCC = 13 V
Switching energy losses at turn-off	W_{OFF}		TBD		uJ	RL = 13 Ω, VCC = 13 V
Protection and diagnostics						
DC short-circuit current	I_{limH}	1.8	2.5	3	A	VDS = 13 V, VS = VIN = 5V
Shutdown temperature	TTSD	150	175	200	°C	
Reset temperature	TR	T_{RS} + 1	T_{RS} + 5		°C	
Thermal reset of STATUS	TRS	135			°C	
Thermal hysteresis (TTSD- TR)	THYST		7		°C	
Dynamic temperature	ΔTj		40		K	Tj =-40°C, VCC = 13V
Dynamic temperature hysteresis	ΔTj(HYS)		15		K	

5.2. Typical Performance Characteristics

5.2.1. True table

Conditions	*Input*	*Drain*	*Status*
Normal operation	L	H	H
	H	L	H
Current limitation	L	H	H
	H	X	H
Over-temperature limitation	L	H	H
	H	H	L
VDD under-voltage	L	H	X
	H	H	X
Open-drain detection	L	L	L
	H	L	H

5.2.2. Electrical characteristics curves

6. Protections

6.1. Current limitation

NSD11416-Q1 has current limitation to protect the silicon and bonding wire in case of overload or short circuit to ground.

6.2. Thermal shutdown and thermal swing

This device has both absolute and dynamic temperature protection. There are two thermal sensors on the controller and the MOSFET, the one on the MOSFET is the hottest and the one on the controller is the coldest. The absolute temperature protection is to shutdown the MOSFET when the hottest junction temperature exceeds the T_{TSD}, and the dynamic temperature protection is also to shutdown the MOSFET when the temperature difference between the hottest and the coldest exceeds ΔTj.

7. Application Information

Figure 3. NSD11416-QSPR(SO-8) application schematic

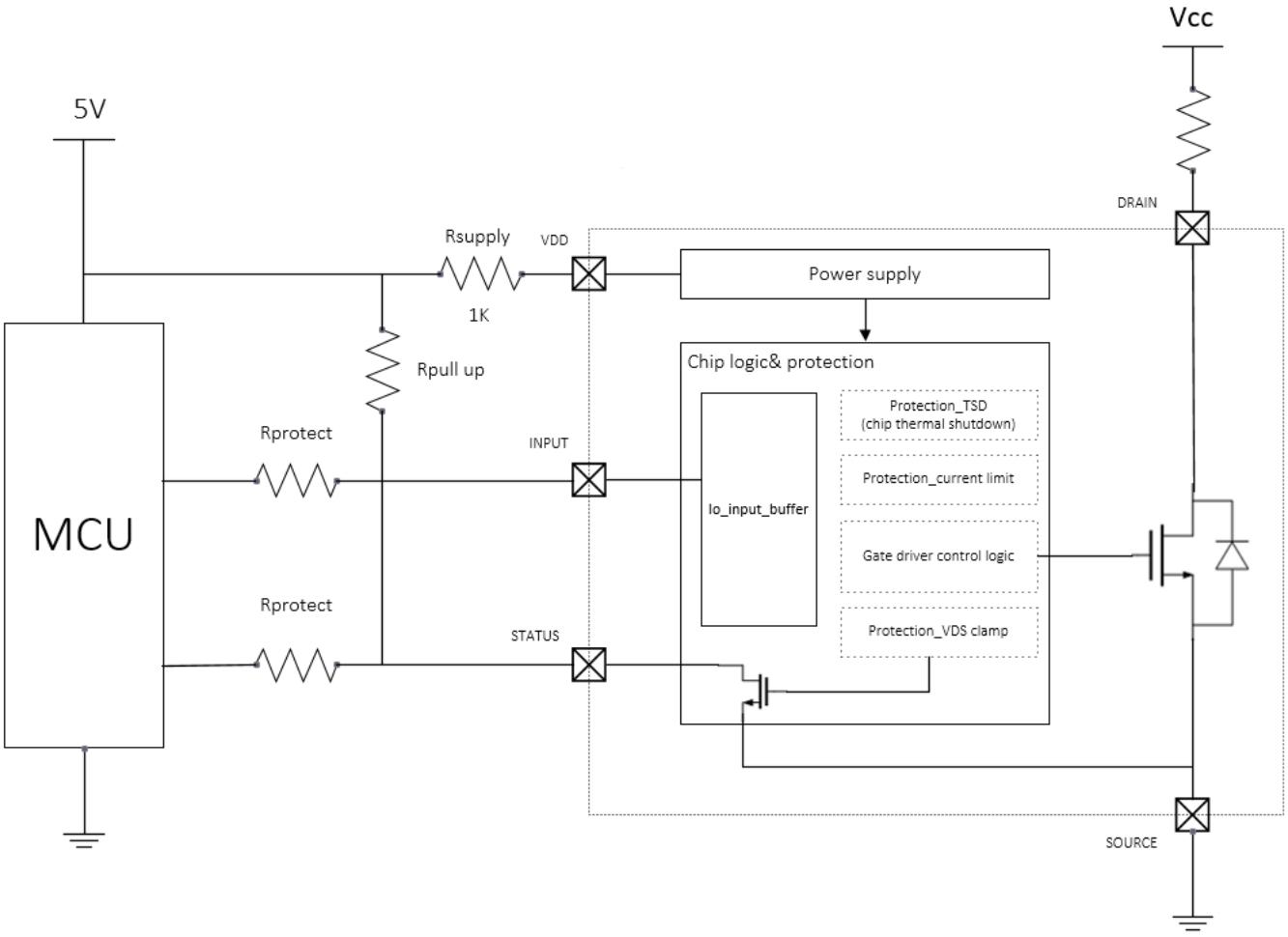
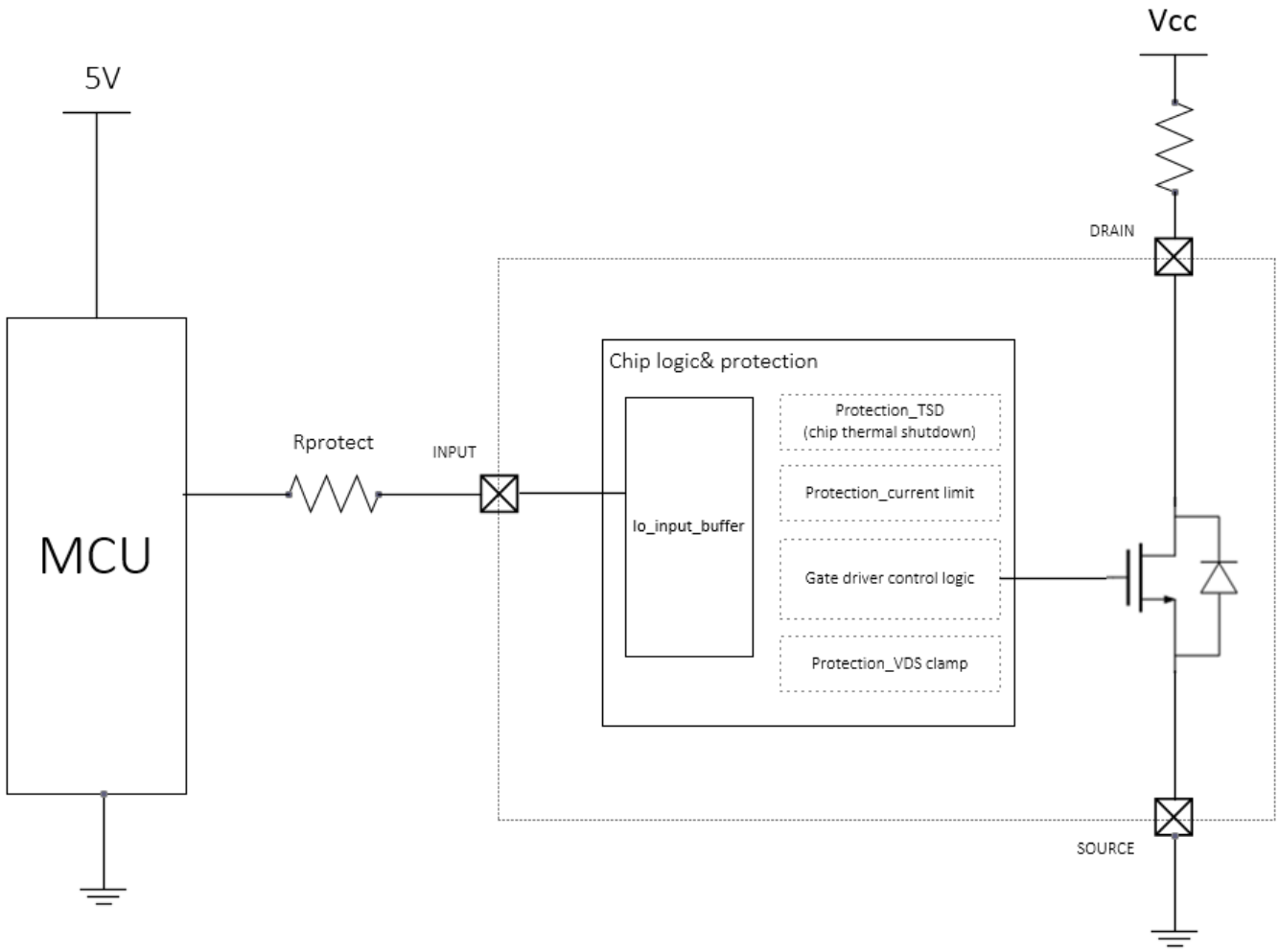


Figure 4. NSD11416-QSTBR(SOT223) application schematic



7.1. MCU I/O protection

NSD11416 has Zener diodes inside for ESD protection and the intrinsic NPN parasitic bipolar, so that resistors for protection are necessary in series with the digital inputs to limit the current to protect MCU I/Os during transient and reverse battery conditions.

The value of resistors for protection can be calculated by the formula as shown below:

$$\frac{V_{ICL}}{I_{latchup}} \le R_{prot} \le \frac{V_{MCU\_OUT} - V_{IH}}{I_{IH\max}}$$

Where V_{ICL} is reverse clamp voltage of NSD11416, $I_{latchup}$ is the MCU I/O latch up current, V_{MCU_OUT} is the output voltage of MCU I/O, V_{IH} is the High-level input voltage of NSD11416, I_{IH} is the high level input current.

Let:

$I_{latchup} \ge 20mA$; $V_{MCU\_OUT} \ge 4.5V$, so $35\Omega \le R_{prot} \le 100k\Omega$, the recommended value is 1kΩ. The supply resistor is the same.

7.2. The value of STATUS pull up resistor

Because the STATUS pin is open drain output, a pull up resister is needed to fix the high voltage during normal operation. When the fault occurs, the voltage level of STATUS is pulled down by the internal MOSFET on. The value of pull up resistor can be calculated by the formula as shown below:

$$(\frac{V_{pull-up}}{V_{OL}}-1)\bullet R_{on} < R_{pull-up} < \frac{V_{pull-up}-V_{OH}}{I_{leak}}$$

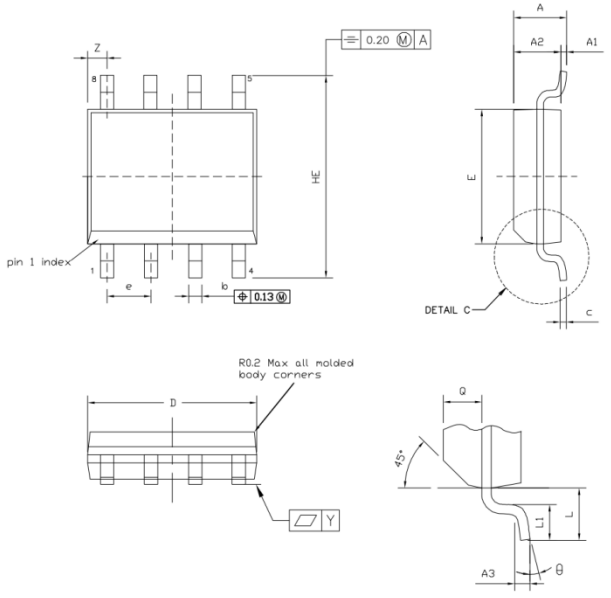
Where V_{pullup} is the minimum of pull-up supply, V_{OL} is the maximum of MCU logic low, R_{on} is the on resistance of the MOSFET of STATUS pin, V_{OH} is the minimum of MCU logic high, I_{leak} is the maximum leakage current of STATUS pin.

Let:

V_{pullup} = 4.5V;R_{on} = V_{STAT}/I_{STAT} = 500Ω, V_{OL} = 0.9V; V_{OH} = 2.1V; I_{leak} = 10uA, so 2kΩ ≤ R_{pullup} ≤ 240kΩ.

8. Package Information

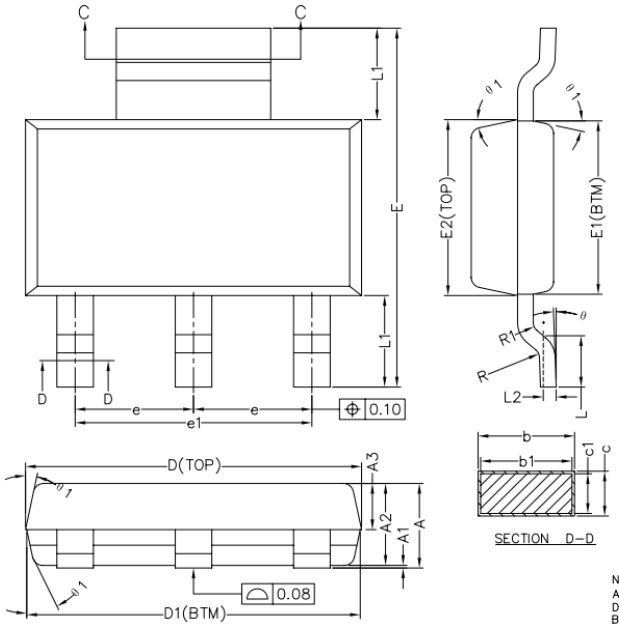
8.1. SO-8



* CONTROLLING DIMENSION : MM

SYMBOL	MILLIMETER		
	MIN.	NOM.	MAX.
A	---	---	1.75
A1	0.10	---	0.25
A2	1.25	1.35	1.45
b	0.33	0.38	0.49
c	0.19	0.20	0.25
D	4.80	4.90	5.00
E	3.80	3.90	4.00
Q	0.60	0.65	0.70
HE	5.80	6.00	6.20
e	1.27 BSC		
L	1.05 BSC		
L1	0.40	0.64	1.00
Y	---	0.10	---
Z	0.3	0.5	0.7
A3	0.25 BSC		
θ	0°	5°	8°

8.2. SOT223



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.80
A1	0.02	–	0.10
A2	1.50	1.60	1.70
A3	0.80	0.90	1.00
b	0.67	–	0.80
b1	0.66	0.71	0.76
b2	2.96	–	3.09
b3	2.95	3.00	3.05
c	0.30	–	0.35
c1	0.29	0.30	0.31
D	6.48	6.53	6.58
D1	6.43	6.48	6.53
E	6.80	–	7.20
E1	3.30	3.38	3.48
E2	3.33	3.43	3.53
e	2.25	2.30	2.35
e1	4.50	4.60	4.70
L	0.80	1.00	1.20
L1	1.78REF		
L2	0.25BSC		
R	0.10	–	–
R1	0.10	–	–
θ	0°	–	8°
θ 1	10°	12°	14°

NOTES:
ALL DIMENSIONS REFER TO JEDEC STANDARD TO261-AA
DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS,
BODY LENGTH INCLUDING MOLD PROTRUSIONS SHALL NOT EXCEED 6.7mm.

9. Order Information

Part Number	*Package*
NSD11416-QSPR	SO-8
NSD11416-QSTBR	SOT223

10. Revision history

Revision	Description	Date
0V1	Initial version	2022/07
0V2	Second version	2022/9/30
0V3	Third version	2022/11/28