40V, 160mΩ, Quad-Channel Smart High-Side Switch

1 FEATURES

- Automotive AEC-Q100 Grade 1 Qualified
- Wide V_{IN} Range: 4V to 40V
- Quad-Channel, 160mΩ
- Individual EN Control for Each Channel
- Ultra-low Standby Current, Typical 1.3μA
- Precise Current Limit
- Two Versions for Multiple Applications
  - Version A: Individual Diagnostics Output
  - Version B: Accurate Current Sensing
- Robust Protection
  - Output Short to GND Protection
  - Inductive Load Negative Voltage Clamp
  - Loss-Of-GND and Loss-Of-Power Protection
  - Over Temperature Protection
- Full Diagnostics
  - Overcurrent and Short-to-Ground Detection
  - Output Short to Battery Detection
  - Open Load Detection
- Operating Junction Temperature -40˚C To 150˚C
- Thermally Enhanced TSSOP-EP28

2 APPLICATIONS

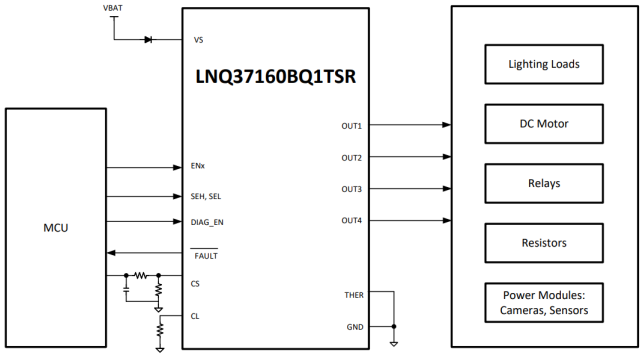
- Multichannel LED Drivers
- Multichannel Relay, Solenoid Drivers
- General Resistance, Capacitance, and Inductance Load Switch
- Multichannel High-Side Switches for Automotive Electronic Module

3 DESCRIPTION

LNQ37160Q1 is a Quad-Channel smart high-side switch with four integrated 160mΩ power MOSFETs that can be independently enabled. The device has full protection functions, including an external adjustable current limit, output short circuit protection, latching off or automatic restart over temperature protection and inductive load negative voltage clamp.

LNQ37160Q1 has full detection and diagnostics functions such as over current, output short to GND, open load, output short to battery, and over temperature. LNQ37160AQ1TSR has individual diagnostics and fault report output for each channel. LNQ37160BQ1TSR has global fault report output for four channels, and it also integrated accurate current sense mirror to output the current information of the selected channel. With this current sense feature, the system can distinguish the specific fault channel by selecting SEL and SEH pin.

LNQ37160BQ1TSR Typical Application Diagram



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4 REVISION HISTORY

Version	Change Description	Date
1.0	Initial Version	2023/5/31

5 PRODUCT INFORMATION

Part Number	IC Package	MSL Peak-Temp (1)	Material	Package	Package Qty	Top Marking (2)
LNQ37160AQ1TSR	TSSOP-EP28	Level-3-260C	RoHS	Tape & Reel	3000	Q37160A
LNQ37160BQ1TSR	TSSOP-EP28	Level-3-260C	RoHS	Tape & Reel	3000	Q37160B

(1) MSL (Moisture Sensitivity Level) is based on JEDEC industrial classification, and the tabled temperature is the maximum solder temperature.

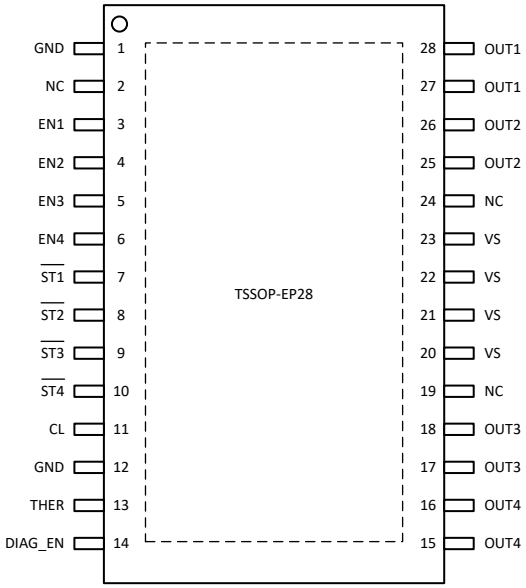
(2) There may be additional marking relates to the lot number or date code on the device.

6 PIN CONFIGURATION AND FUNCTION

6.1 Pin Configuration

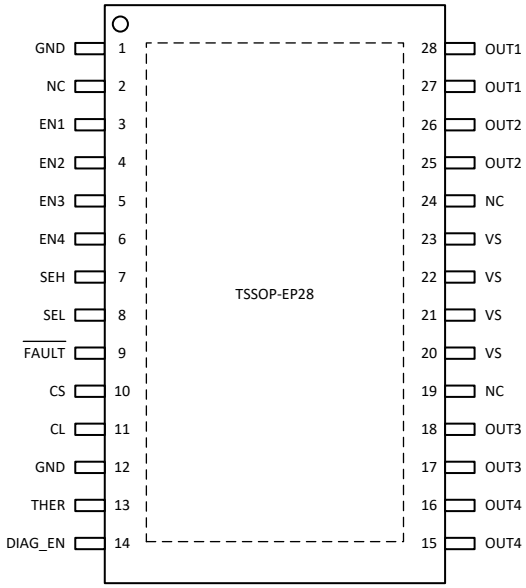
6.1.1 LNQ37160AQ1TSR Pin Configuration

LNQ37160AQ1TSR TSSOP-EP28 Top View



6.1.2 LNQ37160BQ1TSR Pin Configuration

LNQ37160BQ1TSR TSSOP-EP28 Top View



6.2 Pin Functions

Name	PIN Number		Type	Description
	LNQ37160 AQ1TSR	LNQ37160 BQ1TSR		
GND	1,12	1,12	Ground	Device GND.
NC	2,19,24	2,19,24	-	No internal connection.
EN1	3	3	Input	Enable pin for CH1, internal pulldown.
EN2	4	4	Input	Enable pin for CH2, internal pulldown.
EN3	5	5	Input	Enable pin for CH3, internal pulldown.
EN4	6	6	Input	Enable pin for CH4, internal pulldown.
$\overline{ST1}$	7	-	Output	Diagnostic output for CH1 (open drain), low level for fault.
$\overline{ST2}$	8	-	Output	Diagnostic output for CH2 (open drain), low level for fault.
$\overline{ST3}$	9	-	Output	Diagnostic output for CH3 (open drain), low level for fault.
$\overline{ST4}$	10	-	Output	Diagnostic output for CH4 (open drain), low level for fault.
SEH	-	7	Input	CS channel-selection high bit, internal pulldown.
SEL	-	8	Input	CS channel-selection low bit, internal pulldown.
$\overline{FAULT}$	-	9	Output	Global fault report (open drain), low level output for any channel fault.
CS	-	10	Output	Current-sense output, sense channel is selected by SEL and SEH.
CL	11	11	Output	Connect a resistor to device GND to adjust current limit.
THER	13	13	Input	Over temperature protection mode control, internal pulldown. Latch off when THER=H, auto restart when THER=L.
DIAG_EN	14	14	Input	Enable pin for diagnostics, internal pulldown. High level to enable diagnostics function.
OUT4	15,16	15,16	Output	CH4 output.
OUT3	17,18	17,18	Output	CH3 output.
VS	20,21,22,23	20,21,22,23	Power	Power supply, connect a 4.7μF ceramic capacitor and a 0.1uF decoupling capacitor to GND is recommended.
OUT2	25,26	25,26	Output	CH2 output.
OUT1	27,28	27,28	Output	CH1 output.
Thermal Pad				Connect to device GND is recommended.

7 SPECIFICATIONS

7.1 Absolute Maximum Ratings

Over operating ambient temperature range (unless otherwise noted).(1)(2)

Parameters	Conditions	Min	Max	Unit
Supply Voltage		-0.3	48	V
Voltage on ENx, DIAG_EN, SEL, SEH , and THER pins		-0.3	6.5	
Voltage on $\overline{\text{STx}}$, $\overline{\text{FAULT}}$ pins		-0.3	6.5	
Voltage on CS pin		-2.7	6.5	
Voltage on CL to pin		-0.3	6.5	
Reverse current on GND pin		-	50	mA
	t<120s	-	250	
Input current on ENx, DIAG_EN, THER, SEL, SHE pins		-1	2	
	Reverse polarity condition, t<120s	-1	10	
Input current on $\overline{\text{STx}}$, $\overline{\text{FAULT}}$ pins		-1	10	
Output current on CS pin		-2	25	
	Reverse polarity condition, t<120s	-100	-	
Output current on CL pin		-1	4	
Inductive load switch-off energy dissipation, single pulse, single channel(3)		-	21	mJ
Operating Ambient Temperature		-40	125	˚C
Junction Temperature		-40	150	
Storage Temperature		-65	150	

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to the ground plane.

(3) Test condition: V_{VS} = 13.5V, I_L = 2.5A, T_J(initial) = 150℃. Value specified by design, not subject to production test.

7.2 ESD Ratings

Parameters			Value	Unit
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 (1)	All pins except VS, OUTx, GND	±4000	V
		Pins VS, OUTx, GND	±5000	
	Charged device model (CDM), per AEC Q100-011	All pins	±750	

(1) The human-body model is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each terminal.

7.3 Recommended Operating Conditions

Parameters	Min	Max	Unit
VS	4	40	V
ENx, $\overline{STx}$, SEH, SEL, DIAG_EN, $\overline{FAULT}$, THER	0	5	
Nominal DC load current	0	2.5	A
Operating Ambient Temperature	-40	125	˚C
Junction Temperature	-40	150	˚C

7.4 Package Thermal Parameters

Parameter		TSSOP-EP28	Units
$R_{\theta JA}$(1)	Junction-to-Ambient Thermal Resistance	36.0	˚C/W
ψ_{JT}(1)	Junction-to-Top Characterization Parameter	3.7	˚C/W
$R_{\theta JA\text{-}EVM}$	Junction-to-Ambient Thermal Resistance	18.0	˚C/W

(1) Measurements are based on standard 2s2p PCB defined in JESD 51-7 2s2p， under no wind, 2W loss, and 25 ˚C ambient temperature. The value of $R_{\theta JA}$ is a system-level parameter that depends strongly on PCB layout and heat dissipation conditions. $R_{\theta JA}$ on LEN EVM can be much smaller under the same environment.

7.5 Electrical Characteristics

Unless otherwise stated, the minimum and maximum limits apply over the input voltage range of 5V≤VS≤40V, operating junction temperature range of -40˚C - 150˚C. Typical values are measured at 25˚C and represent the most likely norm. The default conditions apply: $I_{CL(ext\_set)}$ = 3A.

SYMBOLS	PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage						
$V_{VS(nom)}$	Nominal operating voltage		4		40	V
$V_{VS(uvr)}$	Undervoltage turn on	V_{VS} rise up	3.50	3.70	4.00	V
$V_{VS(uvf)}$	Undervoltage shutdown	V_{VS} falls down	3.10	3.30	3.50	V
$V_{VS(uv,hys)}$	Undervoltage shutdown, hysteresis			0.4		V
Operating Current						
$I_{(op)}$	Normal operating Current	V_{VS} = 13.5 V, V_{ENx} = 5 V, V_{DIAG_EN}= 0 V, I_{OUTx}= 0.5 A, current limit = 2 A， all channels on		3.5	8.0	mA
$I_{(off)}$	Standby Current	V_{VS} = 13.5 V, V_{ENx} = V_{OUTx} = V_{DIAG_EN} = V_{CS} = V_{CL}= THER = 0 V, T_J = 25 °C		1.3	2.0	µA
		V_{VS} = 13.5 V, V_{ENx} = V_{OUTx} = V_{DIAG_EN} = V_{CS} = V_{CL}= THER = 0 V, T_J = 125 °C			10	
$I_{off(diag)}$	Standby Current with diagnostic enabled	V_{VS} = 13.5 V, V_{ENx} = 0 V, V_{DIAG_EN} = 5 V, V_{VS} – V_{OUTx} > $V_{(ol,off)}$, not in open-load mode			5	mA
$t_{(off,deg)}$	Standby mode deglitch time	V_{VS} = 13.5 V, EN from high to low, if deglitch time > $t_{(off,deg)}$, the device enters into standby mode.	10.0	12.5	15.0	ms
$I_{lkg(out)}$	Output leakage current in off-state	V_{VS} = 13.5 V, V_{DIAG_EN} = V_{ENx} = V_{OUTx} = 0 V			3	uA
Power Stage						
$r_{DS(on)}$	On-state resistance	V_{VS} = 13.5 V, T_J = 25 ˚C		170		mΩ
		V_{VS} = 13.5 V, T_J = 150 ˚C			330	mΩ
$V_{DS(CLAMP)}$	Drain-to-source internal clamp voltage		44	50	56	V
$I_{CL(int)}$	Internal current limit(1)	Internal current limit value, CL pin connected to GND	5.00	6.67	8.34	A
$I_{CL(TSD)}$	Current limit during thermal shutdown(1)	Internal current limit value under thermal shutdown		4.5		A
		External current limit value under thermal shutdown. The percentage of the external current limit setting value.		70		%

Electrical Characteristics (Continued)

Reverse Diode Characteristics						
V_F	Drain-source diode voltage	ENx = 0 V， I_{OUTx} = -0.15 A	0.30	0.78	1.00	V
$I_{R(1)}$	Continuous reverse current from source to drain(1)	t< 60 s, V_{ENx} = 0 V， T_J = 25 ˚C, output short to battery, single channel reversed.		2.5		A
$I_{R(2)}$	Continuous reverse current from source to drain(1)	t< 60 s, V_{ENx} = 0 V， GND pin is connected 1kΩ resistor in parallel with diode. T_J = 25 ˚C. Reverse-polarity condition, all channels reversed.		2		A
Current Limit						
$V_{CL(th)}$	Current limit internal threshold			0.8		V
$K_{(CL)}$	Current-limit ratio			2500		
Current Sense (LNQ37160BQ1TSR)						
$K_{(CS)}$	Current-sense ratio			300		
$dK_{(CS)}/ K_{(CS)}$	Current-sense accuracy, (I_{CS} ×$K_{(CS)}$ – I_{OUTx}) × 100 /I_{OUTx}	V_{VS} = 13.5 V, I_{OUTx} ≥ 5 mA	-80		80	%
		V_{VS} = 13.5 V, I_{OUTx} ≥ 25 mA	-18		18	%
		V_{VS} = 13.5 V, I_{OUTx} ≥ 50 mA	-10		10	%
		V_{VS} = 13.5 V, I_{OUTx} ≥ 100 mA	-6		6	%
		V_{VS} = 13.5 V, I_{OUTx} ≥ 0.5 A	-3		3	%
$dK_{(CL)}/ K_{(CL)}$	External current limit accuracy(2), (I_{OUTx} – I_{CL} ×$K_{(CL)}$) × 100/ (I_{CL} ×$K_{(CL)}$)	V_{VS} = 13.5 V, $I_{CL(ext\_set)}$ ≥ 0.25 A	-60		60	%
		V_{VS} = 13.5 V, $I_{CL(ext\_set)}$ ≥ 0.5 A	-35		35	
		V_{VS} = 13.5 V,1 A ≤ $I_{CL(ext\_set)}$ ≤ 5 A	-20		25	
$V_{CS(lin)}$	Linear current-sense voltage range(1)	V_{VS} ≥ 6.5 V	0		4	V
		5 V ≤ V_{VS} < 6.5 V	0		V_{VS}-2.5	V
$I_{OUTx(lin)}$	Output-current linear range(1)	V_{VS} ≥ 6.5 V, $V_{CS(lin)}$ ≤ 4 V	0		2.5	A
		5 V ≤ V_{VS} < 6.5 V, $V_{CS(lin)}$ ≤ V_{VS} – 2.5 V	0		2.5	A
$V_{CS(H)}$	Fault current sense voltage range	V_{VS} ≥ 7 V, fault mode, CS open	4.5		5.6	V
		5 V ≤ V_{VS} < 7 V, fault mode, CS open	Min(V_{VS} – 2, 4.5)		5.6	V
$I_{CS(H)}$	Current-sense pin output current	V_{VS} = 13.5 V, V_{CS}= 4.5 V	15		25	mA
$I_{lkg(CS)}$	Current-sense leakage current in disabled mode	V_{VS} = 13.5 V, V_{DIAG_EN} = 0 V T_J= 125 ℃			0.5	uA

Electrical Characteristics (Continued)

Diagnostics						
$V_{(ol,off)}$	Open load detection threshold	V_{VS}= 13.5 V, EN = 0 V, when V_{VS} – V_{OUTx} < $V_{(ol,off)}$, duration longer than $t_{d(ol,off)}$, then open load is detected, off state	1.6		2.6	V
$t_{d(ol,off)}$	Open load detection threshold deglitch time(See Figure 3)	V_{VS}= 13.5 V, EN = 0 V, when V_{VS} – V_{OUTx} < $V_{(ol,off)}$, duration longer than $t_{d(ol,off)}$, then open load is detected, off state	300	550	800	µs
$I_{(ol,off)}$	Off-state output sink current	V_{ENx} = 0 V, V_{DIAG_EN} = 5 V, V_{VS} = V_{OUTx} = 13.5 V, T_J = 150 °C, open load	-75			µA
$t_{CL(deg)}$	Deglitch time when current limit occurs or removes	V_{VS}= 13.5 V, V_{ENx} = V_{DIAG_EN} = 5 V, the deglitch time from current limit toggling /removing to $\overline{FAULT}$, $\overline{STx}$, CS report.	75		175	µs
$I_{lkg(GND\_loss)}$	Output leakage current under GND loss condition	V_{VS}= 13.5 V		110	200	uA
Logic Inputs (ENx, SEH, SEL, DIAG_EN, THER)						
V_{IH}	Input logic high voltage		2			V
V_{IL}	Input logic low voltage				0.8	V
$R_{(logic,pd)}$	Logic-pin pulldown resistor	ENx, SEL, SEH, THER, V_{VS}= 13.5 V, V_{ENx} = V_{SEL} = V_{SEH} = V_{THER} = 5 V	100	175	250	kΩ
		DIAG_EN, V_{VS}= 13.5 V, V_{DIAG_EN} = 5 V	100	175	250	
Logic Outputs ($\overline{STx}$, $\overline{FAULT}$)						
$V_{OL(STx)}$	Status low-output voltage	I_{STx} = 2 mA, LNQ37160AQ1TSR only			0.2	V
$V_{OL(FAULT)}$	Fault low-output voltage	I_{FAULT} = 2 mA, LNQ37160BQ1TSR only			0.2	V
Thermal Shutdown						
$T_{(SD)}$	Thermal shutdown threshold(1)		157	165		˚C
$T_{(SD, rec)}$	Thermal shutdown output recovery(1)	V_{THER} = 0 V		155		˚C
$T_{(SD,rst)}$	Thermal shutdown fault reset threshold(1)			145		˚C
$T_{(sw)}$	Thermal swing shutdown threshold(1)			35		˚C
$T_{(hys)}$	Hysteresis for resetting the thermal shutdown or thermal swing(1)			10		˚C

Electrical Characteristics (Continued)

Switching Characteristics						
$t_{d(on)}$	Turn on delay, ENx rising edge to 10% of V_{OUTx} (See Figure 1)	V_{VS} = 13.5 V, V_{DIAG_EN} = 5 V, I_{OUTx} = 0.5 A, EN rising edge to 10% of V_{OUTx}	30	60	100	µs
$t_{d(off)}$	Turn off delay, ENx falling edge to 90% of V_{OUTx} (See Figure 1)	V_{VS} = 13.5 V, V_{DIAG_EN} = 5 V, I_{OUTx} = 0.5 A, EN falling edge to 90% of V_{OUTx}	30	60	100	µs
dV/dt(on)	Turn on slew rate, V_{OUTx} from 10% to 90%	V_{VS} = 13.5 V, V_{DIAG_EN} = 5 V, I_{OUTx}= 0.5 A	0.10	0.35	0.55	V/µs
dV/dt(off)	Turn off slew rate, V_{OUTx} from 90% to 10%	V_{VS} = 13.5 V, V_{DIAG_EN} = 5 V, I_{OUTx}= 0.5 A	0.10	0.35	0.55	V/µs
$t_{d(match)}$	$t_{d(rise)} - t_{d(fall)}$ (See Figure 1)	V_{VS} = 13.5 V, I_{OUTx} = 0.5 A. $t_{d(rise)}$ is the EN rising edge to V_{OUTx} = 90%.$t_{d(fall)}$ is the EN falling edge to V_{OUTx} = 10%.	-50		50	µs
dv/dt(match)	Slew Rate Matching dV/dt(on)- dV/dt(off) (See Figure 1)	V_{VS} = 13.5 V, V_{DIAG_EN} = 5 V, I_{OUTx}= 0.5 A	-0.15	0	0.15	V/µs
Current Sense Characteristics (See Figure 2)						
$t_{cs(on1)}$	CS settling time from DIAG_EN enabled , DIAG_EN rising edge to 90% of V_{CS}	V_{VS} = 13.5 V, V_{ENx} = 5 V, I_{OUT}= 0.5 A, current limit = 2 A			20	µs
$t_{cs(off1)}$	CS settling time from DIAG_EN disabled, DIAG_EN falling edge to 10% of V_{CS}	V_{VS} = 13.5 V, V_{ENx} = 5V, I_{OUT}= 0.5 A, current limit = 2 A			20	µs
$t_{cs(on2)}$	CS settling time from EN rising edge, EN rising edge to 90% of V_{CS}	V_{VS} = 13.5 V, V_{DIAG_ENx} = 5 V, I_{OUT}= 0.5 A, current limit = 2 A	80	120	150	µs
$t_{cs(off2)}$	CS settling time from EN falling edge, EN falling edge to 10% of V_{CS}	V_{VS} = 13.5 V, V_{DIAG_ENx} = 5 V, I_{OUT}= 0.5 A, current limit = 2 A			20	µs
t_{SEx}	Multi-sense transition delay from channel to channel (See Figure 4)	V_{VS} = 13.5 V, V_{DIAG_EN} = 5 V, current sense output delay when multi-sense pins SEL and SEH transition from channel to channel			50	µs

(1) Value specified by design, not subject to production test.

(2) External current limit accuracy is only applicable to overload conditions greater than 1.5 x the current limit setting and current limit accuracy is only applicable to overload condition at VDS ≥ 5 V.

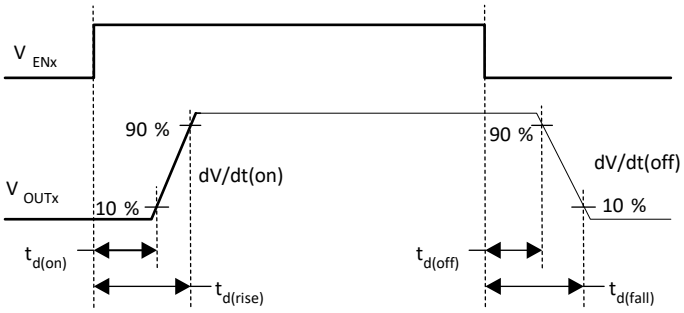


Figure 1. Output Delay Characteristics

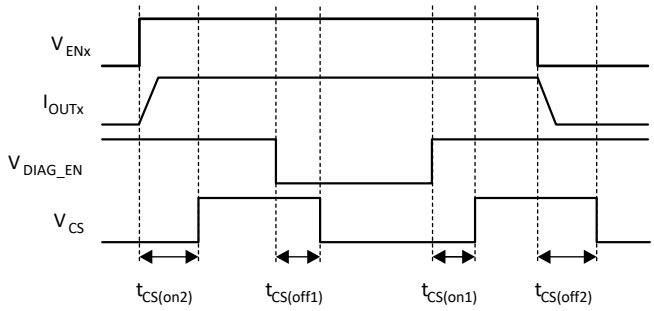


Figure 2. CS Delay Characteristics

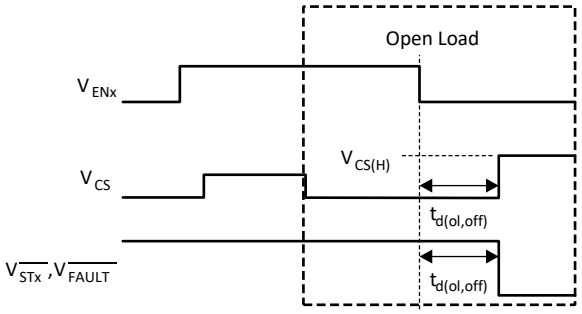


Figure 3. Open-Load Blanking-Time Characteristics

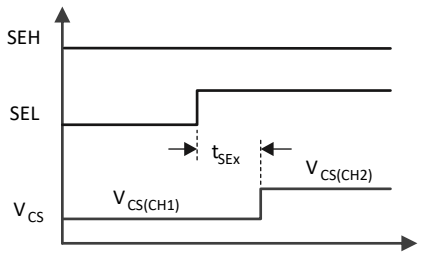
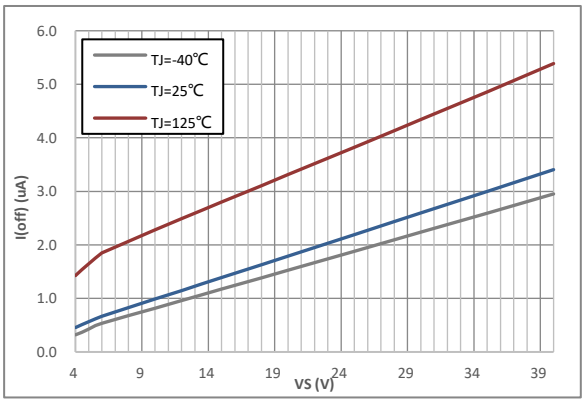


Figure 4. Multi-Sense Transition Delay

7.6 Typical Characteristics

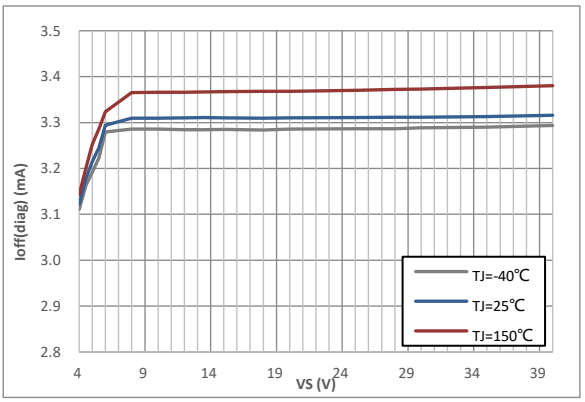
7.6.1 Parameter Curves

Unless otherwise stated, the test conditions are: V_{VS} = 13.5 V, R_{CL}= 620 Ω, TA = 25 ˚C.



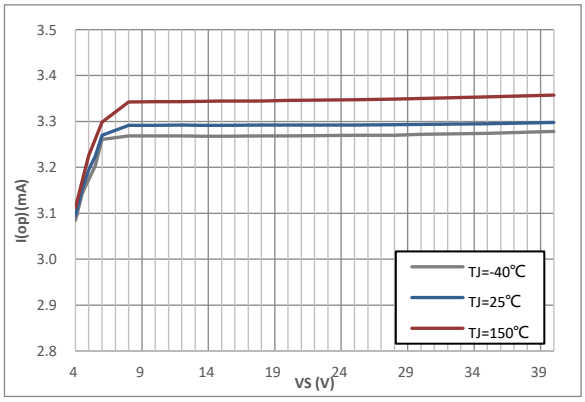
EN = DIAG_EN = 0 V

Figure 5. $I_{(off)}$



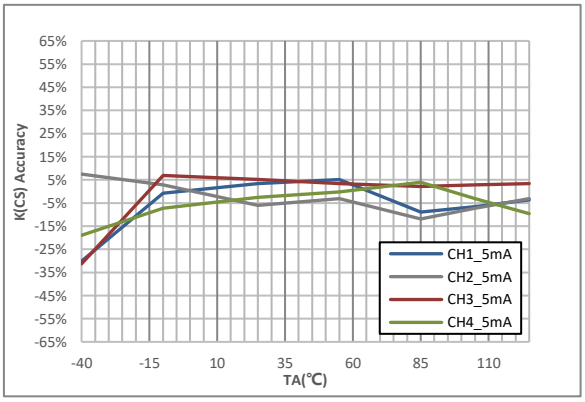
EN = 0 V, DIAG_EN = 5 V

Figure 6. $I_{off(diag)}$



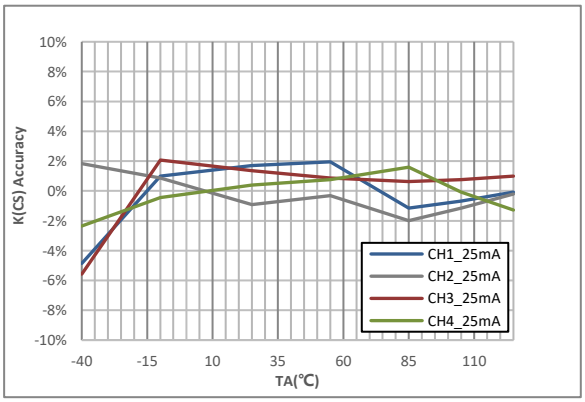
EN = 5 V, DIAG_EN = 0 V

Figure 7. $I_{(op)}$



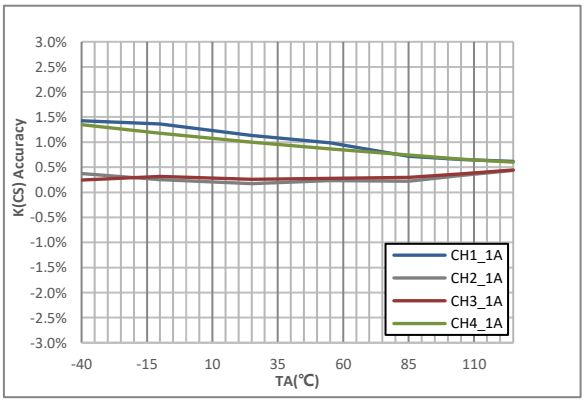
V_{VS} = 13.5 V, I_{OUT} = 5 mA

Figure 8. $K_{(CS)}$ Accuracy vs. Temperature



V_{VS} = 13.5 V, I_{OUT}= 25 mA

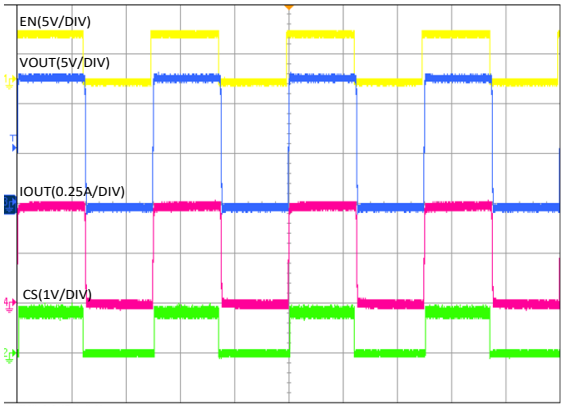
Figure 9. $K_{(CS)}$ Accuracy vs. Temperature



V_{VS} = 13.5 V, I_{OUT} = 1 A

Figure 10. $K_{(CS)}$ Accuracy vs. Temperature

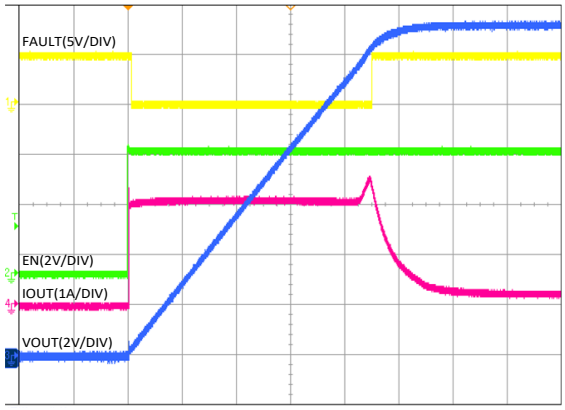
7.6.2 Typical Waveforms



Time (2 ms/DIV)

V_{VS} = 13.5 V, LOAD = 0.5 A, R_{CS} = 475 Ω

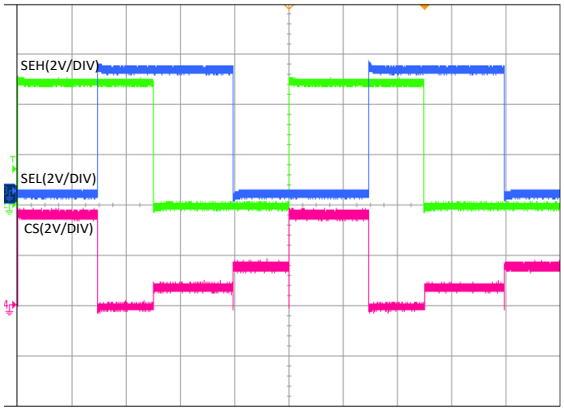
Figure 11. LNQ37160BQ1TSR, Startup/ Shutdown through EN



Time (3 ms/DIV)

V_{VS} = 13.5 V, CL = 2.3 mF, I_{OUT} = 0.2 A, R_{CL} = 1 kΩ

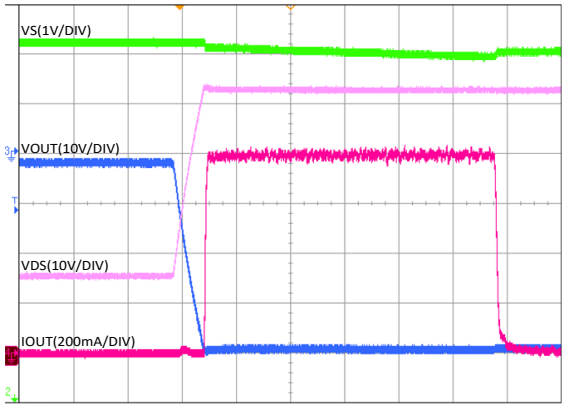
Figure 12. LNQ37160BQ1TSR, Startup with Capacitive Load



Time (2 ms/DIV)

V_{VS} = 13.5 V, R_{CS} = 475 Ω, I_{OUT1} = 1 A, I_{OUT2} = 0.5 A, I_{OUT3} = 2.5 A, I_{OUT4} = 0 A

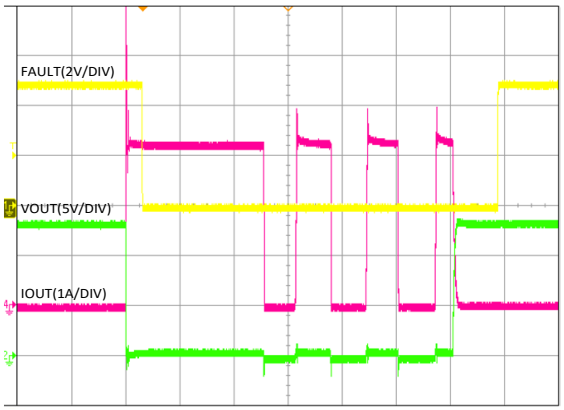
Figure 13. LNQ37160BQ1TSR, Current Sense Channel Transition



Time (200 us/DIV)

V_{VS} = 13.5 V, Single Pulse 45 mJ

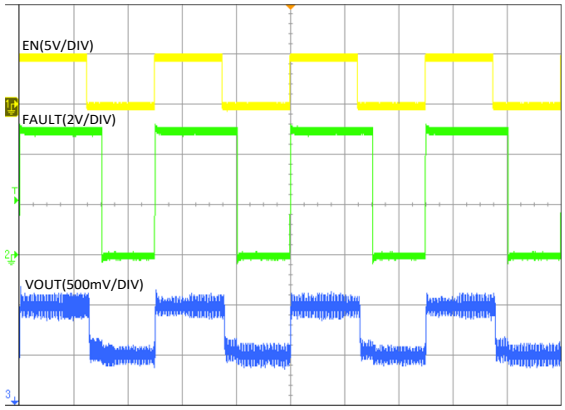
Figure 14. VDS Clamp



Time (500 us/DIV)

V_{VS} = 13.5 V, RCL = 620 Ω

Figure 15. LNQ37160BQ1TSR, Short Protection



Time (12ms/DIV)

V_{VS} = 13.5 V, Connect 20kΩ resistor from OUT to VS

Figure 16. LNQ37160BQ1TSR, Open Load Detect

8 FUNCTIONAL BLOCK DIAGRAM

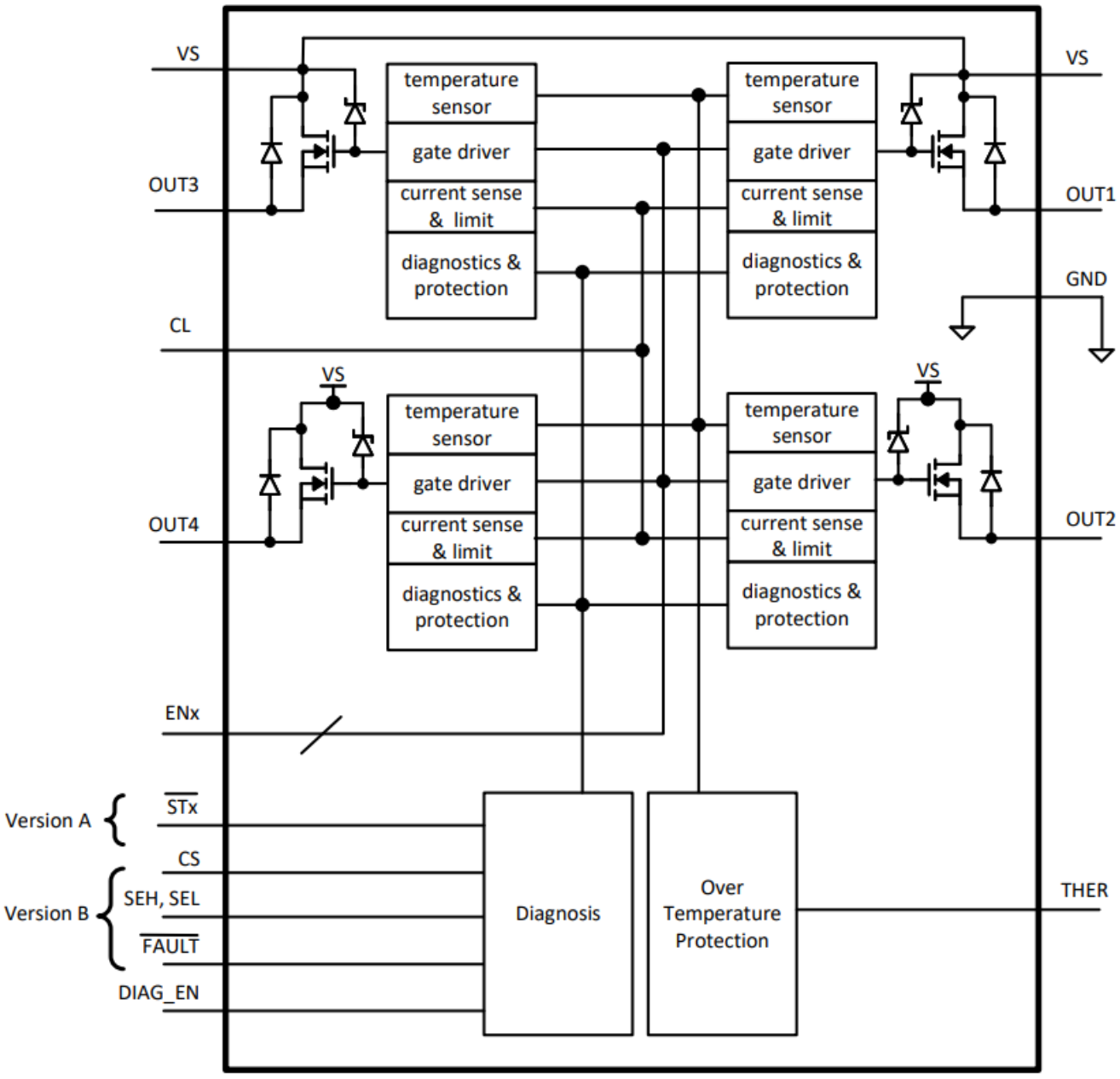


Figure 17. LNQ37160Q1 Functional Block Diagram

9 FUNCTION DESCRIPTION

LNQ37160Q1 is a Quad-Channel smart high-side switch with four integrated 160mΩ power MOSFETs that can be independently enabled. The device has full protection functions, including an external adjustable current limit, output short circuit protection, latching off or automatic restart over temperature protection and inductive load negative voltage clamp.

LNQ37160Q1 has full detection and diagnostics functions such as over current, output short to GND, open load, output short to battery, and over temperature. LNQ37160AQ1TSR has individual diagnostics and fault report output for each channel. LNQ37160BQ1TSR has global fault report output for four channels, and it also integrated accurate current sense mirror to output the current information of the selected channel. With this current sense feature, the system can distinguish the specific fault channel by selecting SEL and SEH pin. LNQ37160Q1 is packaged with thermally enhanced TSSOP-EP28.

9.1 Working Mode

LNQ37160Q1 will start up when VS power up and V_{VS} is higher than the rising UVLO threshold. After startup initialization, the device enters standby state. At this time, if changing the state of EN or DIAG_ EN, the device will enter normal operation state or standby mode with diagnostic function. The working process is shown in the figure below.

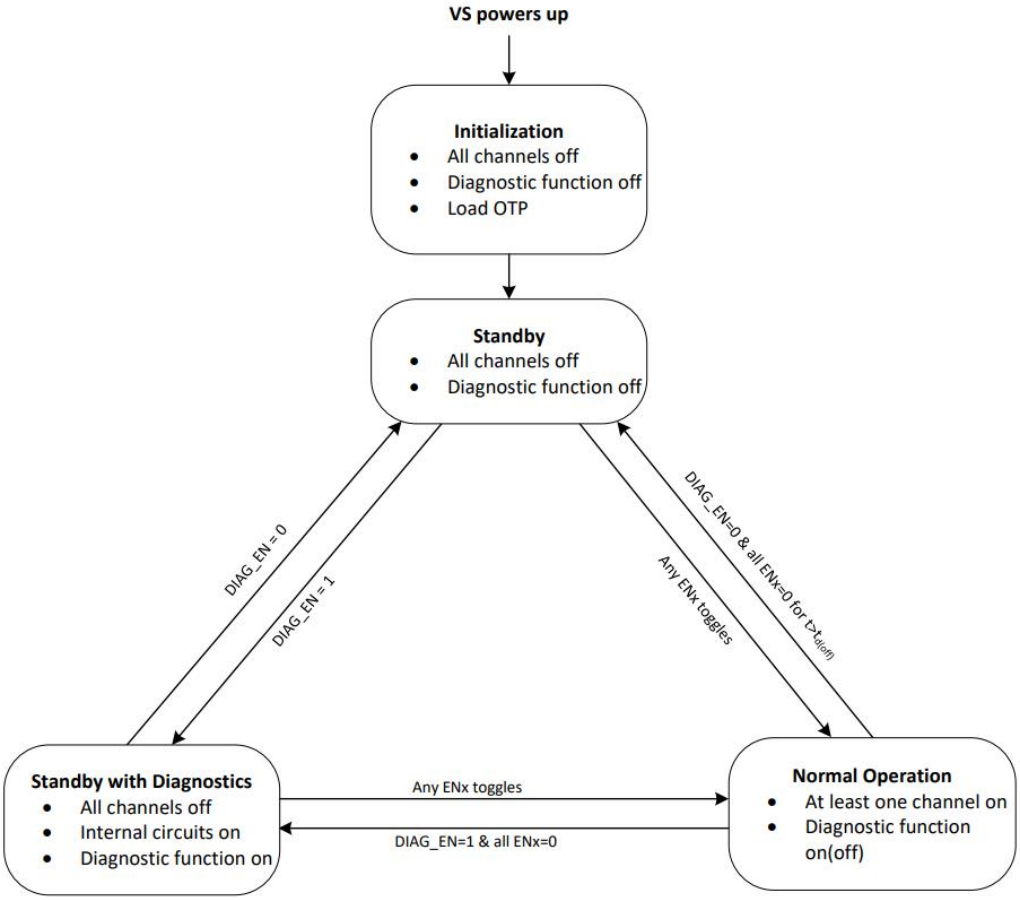


Figure 18. Working Mode Diagram

9.2 Input and Output

9.2.1 Power Supply – VS

VS is the power input for four channels. It is recommended to connect a 4.7μF ceramic capacitor and a 0.1uf decoupling capacitor to GND.

9.2.2 Channel Output – OUTx

OUTx are channel output pin. If the load switch is used to power off-board modules, it is recommended to connect a ceramic capacitor between OUT and GND to strengthen ESD protection capabilities.

9.2.3 Enable Control - ENx

ENx are enable control pins for each channel. When EN voltage level is higher than 2V, the corresponding channel can be turned on. When EN voltage level is lower than 0.8V, the corresponding channel can be shut down.

9.3 Adjustable Current Limit

9.3.1 Current limit during normal operation

LNQ37160Q1 has two current limit thresholds.

- **Internal current limit**
  There is a fixed internal current limit $I_{CL(int)}$. The internal current limit is applicated when the CL pin is tied directly to the device GND.
- **External adjustable current limit**
  The external adjustable current limit is applicated when a current limit resistor R_{CL} is connected between CL and the device GND. Customer can set the current limit value by adjusting R_{CL}. The current limit is determined by the following equation:

$$I_{CL(ext,set)} = \frac{V_{CL(th)} \cdot K_{(CL)}}{R_{CL}}$$

$V_{CL(th)}$ is internal reference voltage, K_{CL} is the ratio of the output current to the current in resistor R_{CL}.

9.3.2 Current limit during thermal shutdown

When current limit occurs, the output current is clamped at the set value and the device heats up due to high power dissipation on the power FET. After the junction temperature hits $T_{(SD)}$, the current limit foldback to $I_{CL(TSD)}$ to reduce the power dissipation.

9.4 Current Sense (LNQ37160BQ1TSR Only)

LNQ37160BQ1TSR CS pin outputs a mirror current proportional to the output current of the selected channel. The current sense proportionality is K_{CS}.

$$K_{(CS)} = \frac{I_{OUTx}}{I_{CS}}$$

A sense resistor is connected between CS and GND, the sense current flow through the sense resistor and the sense voltage V_{CS} is measured by MCU. The value of sense resistor should meet following formula, and the maximum value of $V_{CS(NORMAL)}$ should also be lower than the full scale of MCU ADC.

$$V_{CS(NORMAL)} = I_{CS} \cdot R_{CS} < MAX(V_{CS(lin)})$$

It is recommended add RC filter on MCU port to enhance noise immunity, as shown in Figure 27. RC filtering parameters can be selected according to application timing requirement.

When a fault occurs, a fault voltage $V_{CS(FAULT)}$ is reported at CS pin. $V_{CS(FAULT)}$ is the smaller value of $I_{CS(H)} * R_{CS}$ and $V_{CS(H)}$, as shown in the following formula:

$$V_{CS(FAULT)} = \mathrm{MIN}[I_{CS(H)} \cdot R_{CS},\ V_{CS(H)}]$$

If the actual fault voltage exceeds the maximum rating voltage of the MCU port, a smaller R_{CS} or TVS protection circuit is recommended.

The maximum power dissipation on R_{CS} also occurs on fault condition, as shown in the following formula:

$$P_{RCS} = \mathrm{MIN}[I_{CS(H)}^2 \cdot R_{CS}, V_{CS(H)}^2 / R_{CS}]$$

It is noted that when a reverse polarity occurs, there will be a significant power consumption on the current sense resistor if VS is not blocked by a diode, LEN recommends the use of a large package of current sense resistor.

9.5 Inductive-Load Switching-Off Clamp

When switching off an inductive load, negative voltage will be generated across the inductor, so the output of the switch pulled to negative. If no special control of the negative voltage, the power MOSFET may got damaged. LNQ37160Q1 integrated an internal clamp circuit to limit the negative voltage to $V_{DS(CLAMP)}$ and protect the power MOSFET from damage.

$$V_{DS(CLAMP)} = V_{VS} - V_{OUT}$$

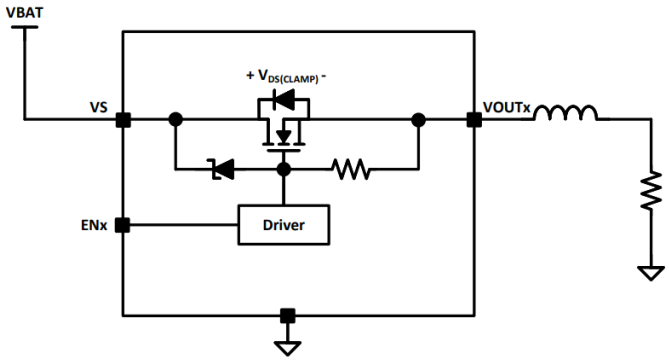


Figure 19. VDS_CLAMP Circuit

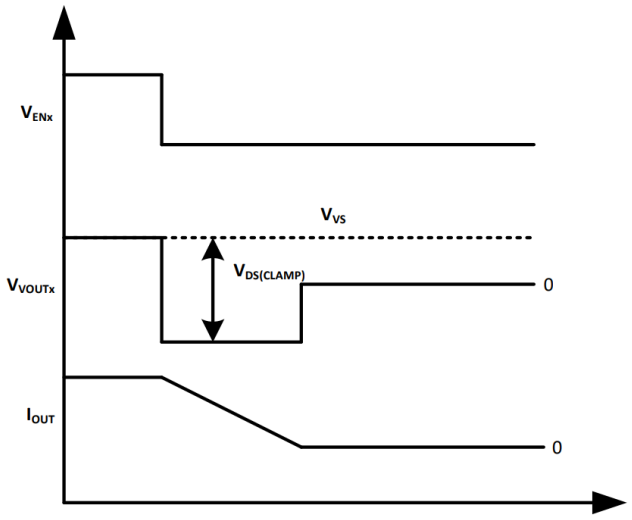


Figure 20. Inductive Load Switching off Diagram

Note that for PWM-controlled inductive loads, the negative voltage stress is repetitive. An external free-wheeling circuit is recommended to protect the device. The circuit is shown in the figure below:

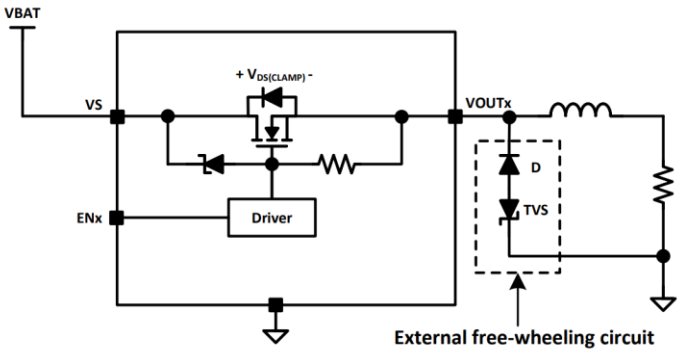


Figure 21. Protection with External Circuit

9.6 Diagnostics and Fault

9.6.1 Diagnostics and Fault Enable - DIAG_EN

DIAG_EN can enable and disable diagnostics and fault function to save power consumption. When DIAG_EN is high, diagnostics and fault function is enabled. When DIAG_EN is low, diagnostics and fault function is disabled, and CS, $\overline{\text{STx}}$ or $\overline{\text{FAULT}}$ are in high impedance output state to save the quiescent current.

9.6.2 Current Sense Channel-selection - SEH and SEL（LNQ37160BQ1TSR）

The current sense channel is selected by SEH and SEL for LNQ37160BQ1TSR. The output current is reduced proportionally and output by CS pin for the selected channel.

SEH	SEL	CHANNEL
L	L	1
L	H	2
H	L	3
H	H	4

9.6.3 Diagnostics and Fault Output - $\overline{STx}/\overline{FAULT}$

LNQ37160AQ1TSR has individual diagnostics and fault output for each channel. When one of the channels has fault, the corresponding $\overline{ST}$ pin changes to low level to indicate fault state.

LNQ37160BQ1TSR has global diagnostics and fault output for four channels. When any channel has fault, $\overline{FAULT}$ pin will change to low level to indicate fault state.

$\overline{STx}/\overline{FAULT}$ are open drain output, an external pull up resistor connected to 3.3V or 5V is necessary.

Diagnostics and fault configuration table is as below when DIAG_EN pin is enabled.

Diagnosis Type	ENx	OUTx	$\overline{STx}/\overline{FAULT}$	CS	THER	Fault Recovery
Normal	L	L	H	0V	-	-
	H	H	H	In linear region	-	-
Overload, short to ground	H	L	L	$V_{CS(FAULT)}$ (2)	-	Auto
Open load(1), short to battery	L	H	L	$V_{CS(FAULT)}$	-	Auto
Thermal shutdown	H	L	L	$V_{CS(FAULT)}$	L	Output auto-retry. Fault recovers when $T_J < T_{(SD,rst)}$ or when ENx toggles.
				$V_{CS(FAULT)}$	H	Latch off and restart when ENx toggles.
Thermal swing	H	L	L	$V_{CS(FAULT)}$	-	Auto

(1) An external pullup is required for open-load detection.

(2) $V_{CS(FAULT)}$ is defined in section 9.4.

9.6.4 Short-to-GND and Overload Detection

A short to GND or overload condition causes overcurrent, If the overcurrent hits the current-limit threshold, the fault is reported out. When the microcontroller gets the fault report, it can handle the overcurrent by turning off the switch. When the overcurrent disappears, the fault report is removed automatically.

9.6.5 Open Load Detection

When DIAG_EN is high level and ENx is low level, open load detection is enabled. A 20kΩ detection resistor is recommended between VS and OUTx to achieve this function. If a load is connected, OUTx is pulled down to GND. But if no load is connected, OUTx will be pulled up close to VS voltage. When the voltage of OUTx meet below formula, the open load fault is reported out.

$$V_{VS} - V_{OUTx} < V_{(ol,off)}$$

9.6.6 Short to Battery Detection

Output short to battery has the same detection mechanism as open-load detection. When DIAG_EN is high level and ENx is low level, if output short to battery, OUTx is equal to or over than VS voltage, $\overline{\text{STx}}/\overline{\text{FAULT}}$ will report fault. Note that when short to battery occurs, the reverse current must be no more than $I_{R(1)}$, otherwise the device may be damaged.

9.7 Robust Protection Fuction

9.7.1 Input UVLO Protection

When V_{VS} is higher than the UVLO rising threshold, the device starts up and enter standby or normal operating mode. When V_{VS} is lower than the UVLO falling threshold, the device shuts down.

9.7.2 Output Short to GND and Over Load Protection

When a short to GND or overload condition occurs, the output current is clamped at the set current limit value, protects the load and the power supply from overstressing. An external resistor is used to set the current limit threshold. The details can refer to section 9.3. The device automatically recovers when the over current condition is removed. The device is AEC-Q100-012 Grade B qualified and has high reliability under short-circuit protection.

9.7.3 Reverse-Current Protection

Reverse current will flow through the device in two conditions:

- **Short to battery:**
  When a short to battery occurs, the reverse current flows through the body diode, $I_{R(1)}$ specifies the upper limit of this reverse current.
- **Reverse polarity:**
  When a reverse polarity occurs, the reverse current flows through the body diode and the device GND pin. $I_{R(2)}$ specifies the upper limit of this reverse current.

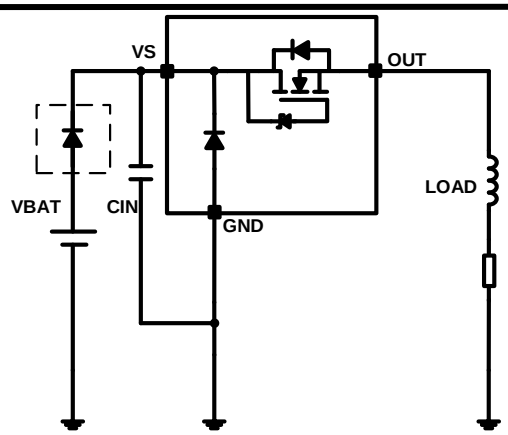


Figure 22. Reverse-Current External Protection, Method 1

LEN recommends two types of external circuitry to protect the device.

- As shown in Figure 22，adding a blocking diode between power supply and the VS pin of device.
- As shown in Figure 23，adding a GND network. The GND network consists of a 1 kΩ resistor and a diode connected in parallel. It is noted that when a reverse polarity occurs，there will be significant power consumption on the 1 kΩ resistor. LEN recommends the use of 1206 package resistors.

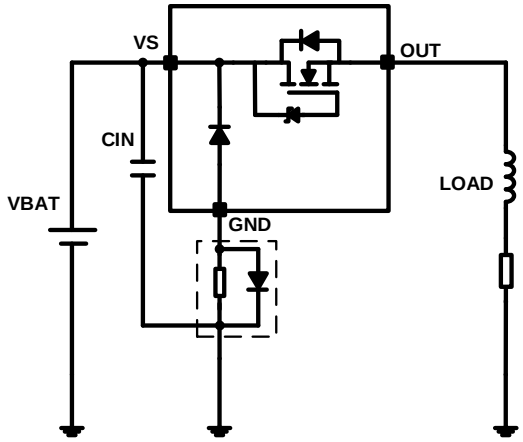


Figure 23. Reverse-Current External Protection, Method 2

9.7.4 Loss-of-GND Protection

LNQ37160Q1 could shut down the output regardless of whether the ENx pin is high or low to protect against loss of device GND and loss of module GND. For inductive loads, LEN recommends adding GND network and external circuitry to better protect the device, as shown in Figure 24.

9.7.5 Loss of Power Supply Protection

For resistive and capacitive loads, LNQ37160Q1 can rapidly shut down the output whether EN is high or low. There is no risk of damaging the device. But for a charged inductive load, the current is driven from all the I/O pins to maintain the

inductance current. The risk of device damaging will increase significantly without external protections. LEN recommends adding GND network and external circuitry to better protect the device, as shown in Figure 24.

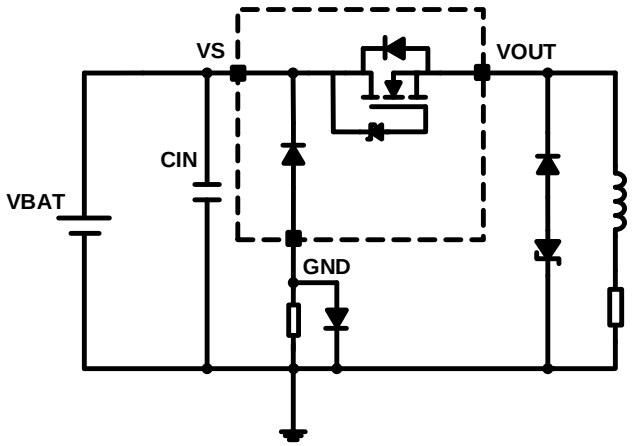


Figure 24. Loss of Power Supply and Loss of GND External Protection for Inductive Load

9.7.6 Over Temperature Protection

There are two over temperature protection behaviors, one is thermal swing, the other is thermal shut down. There is a temperature sensor $T_{(FET)}$ close to the power MOSFET of each channel, and a temperature sensor $T_{(logic)}$ close to the logic circuit. Each channel has individual over temperature protection.

- **Thermal Swing**

When $T_{(FET)}$ is increasing sharply and $T_{(FET)} - T_{(logic)} > T_{(sw)}$, thermal swing activates, then output is turned off shortly. When $T_{(FET)} - T_{(logic)} < T_{(sw)} - T_{(hys)}$, the output automatically recovers. Thermal swing responses rapidly when fast thermal variation occurs, thus prevent chip damage due to excessive local temperature rise.

- **Thermal Shutdown**

When $T_{(FET)}$ is higher than the absolute temperature, that is $T_{(FET)} > T_{(SD)}$, thermal shut down activates. There are two protection mode according to the configuration of THER pin. THER=L, channel output is turned off and automatically recovers when $T_{(FET)} < T_{(SD,\ rec)}$. Fault recovers when $T_J < T_{(SD,rst)}$ or when ENx toggles. THER=H, channel output is latched off and will not restart, unless the related ENx pin is toggled.

Figure 25 shows the two over temperature behaviors after output short to GND.

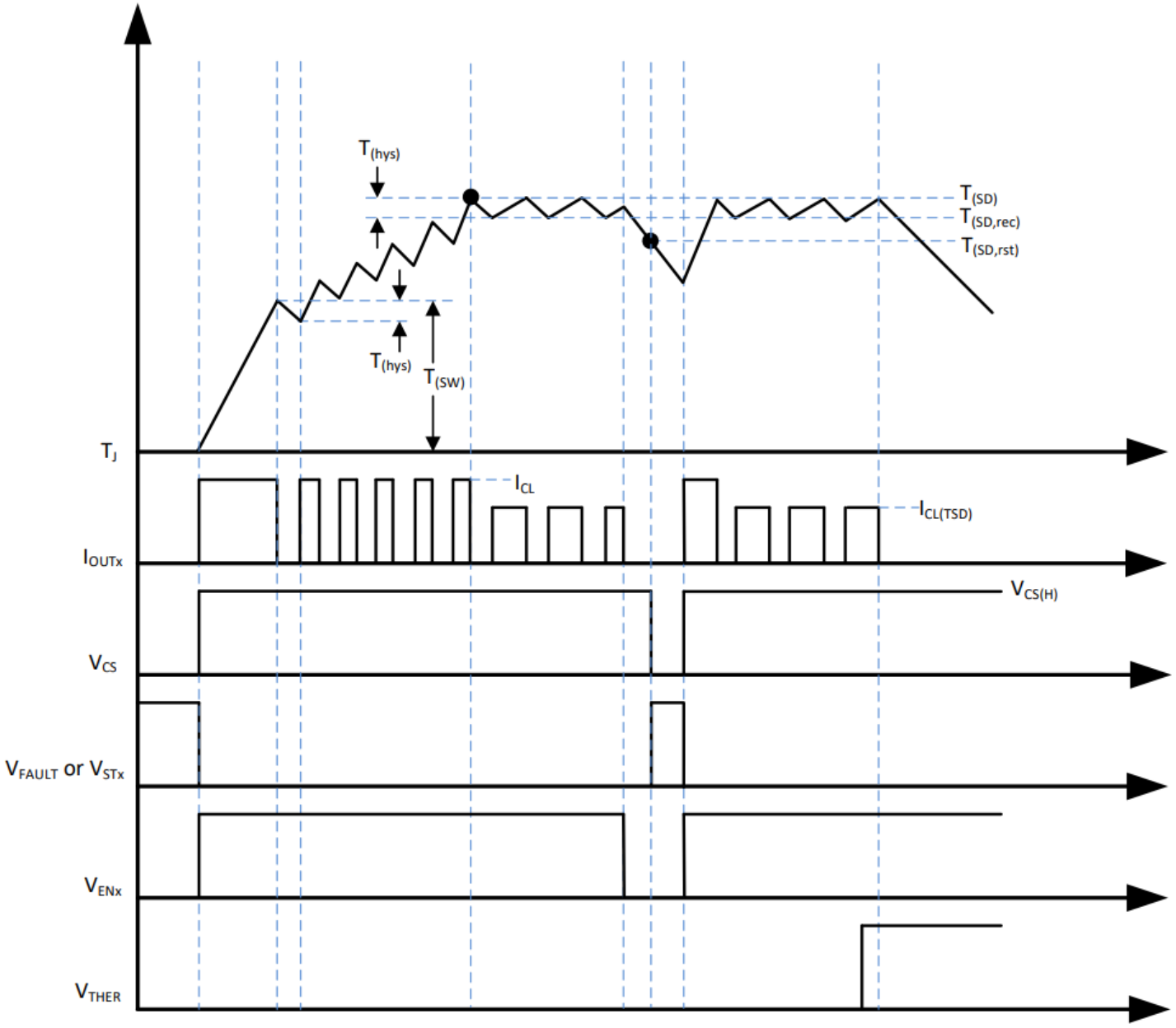


Figure 25. Thermal Behaviors after Output Short to GND

10 APPLICATION INFORMATON

10.1 Typical Application for LNQ37160AQ1TSR

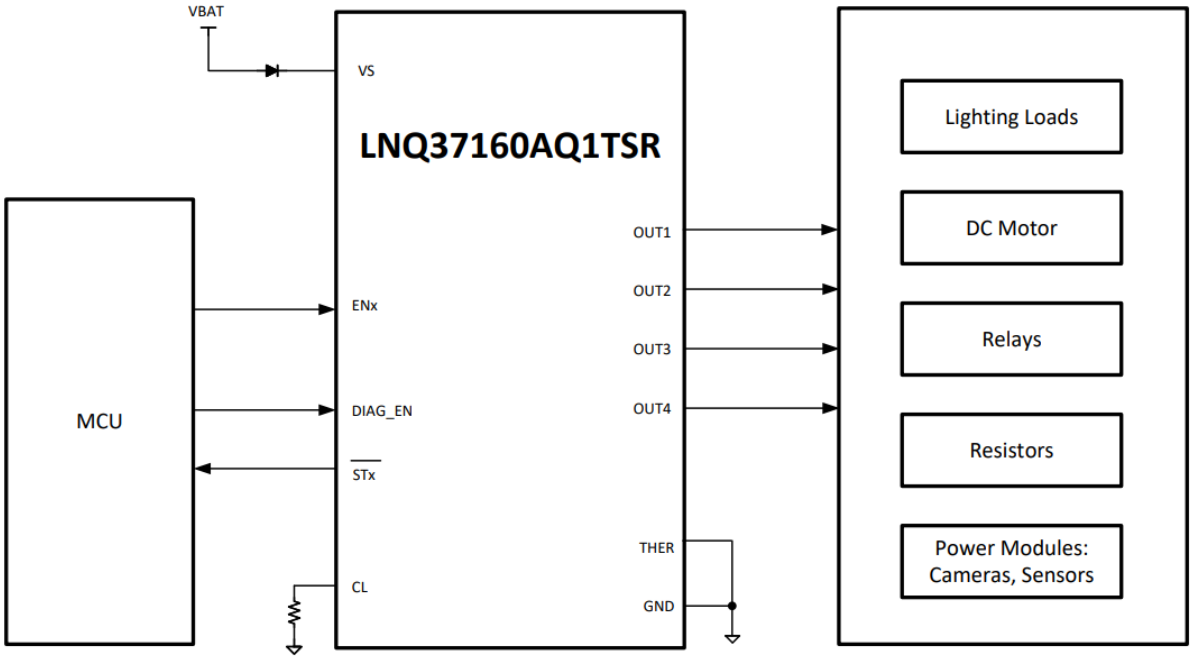


Figure 26. Typical Application for LNQ37160AQ1TSR

10.2 Typical Application for LNQ37160BQ1TSR

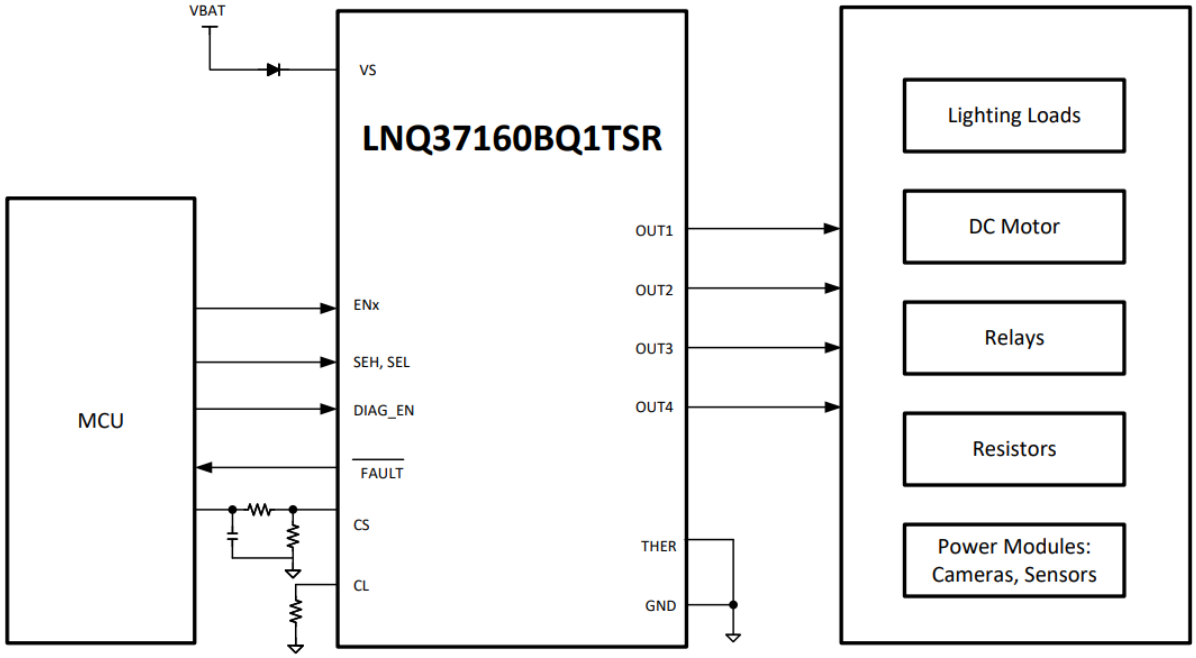
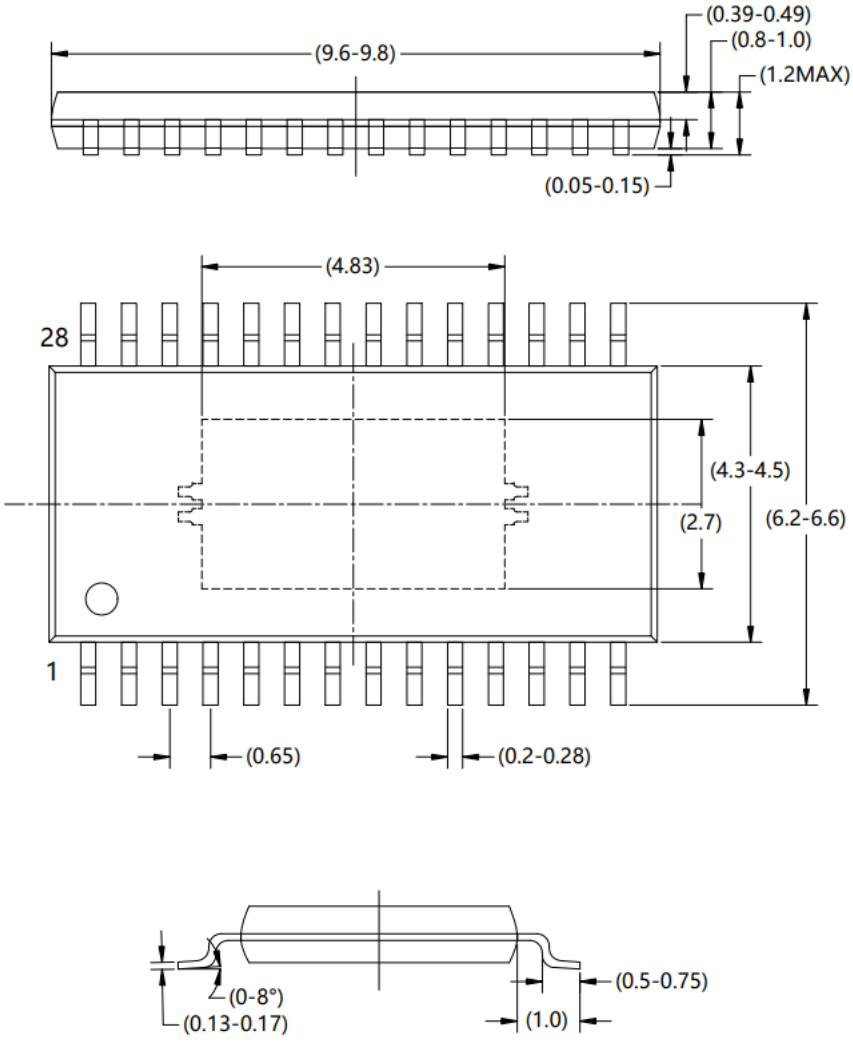


Figure 27. Typical Application for LNQ37160BQ1TSR

11 PACKAGE INFORMATION

11.1 Package Outline



Notes:

1. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

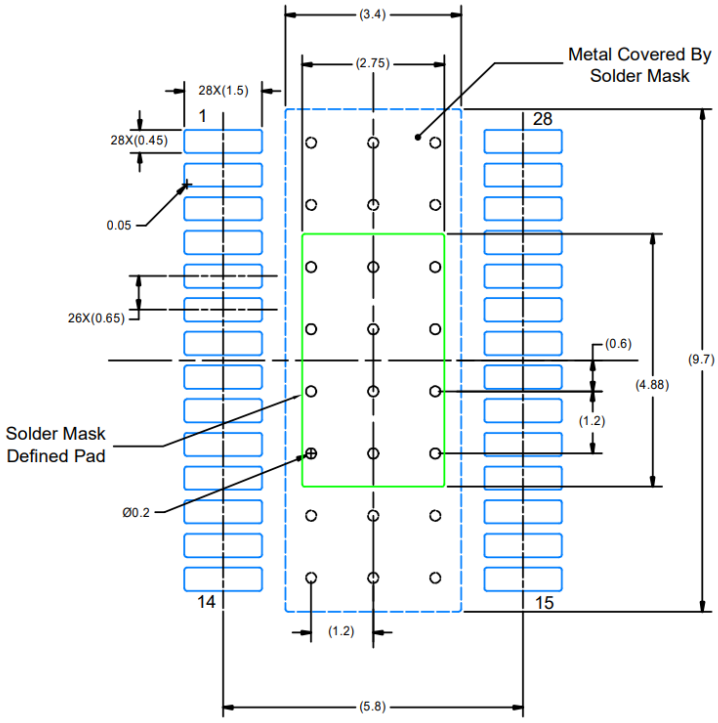
2. Both package length and width does not include mold flash.

3. Unremoved flash between leads & package end flash shall not exceed 0.15mm from bottom body per side.

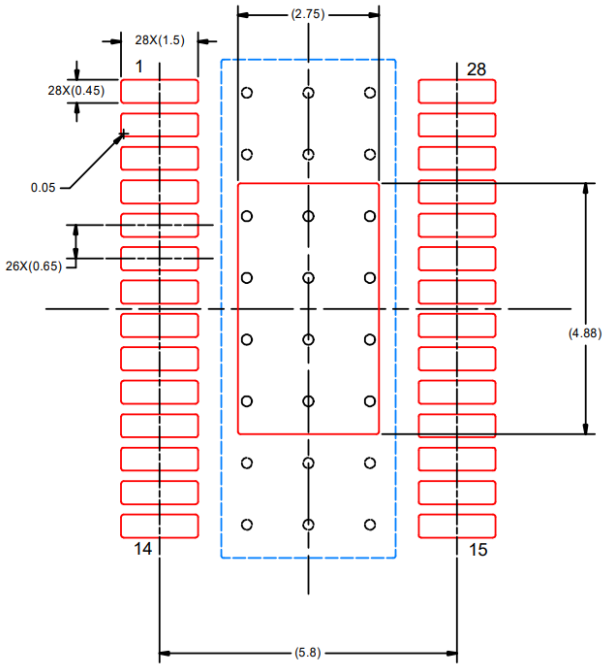
4. Features may not present.

11.2 Footprint Example

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN

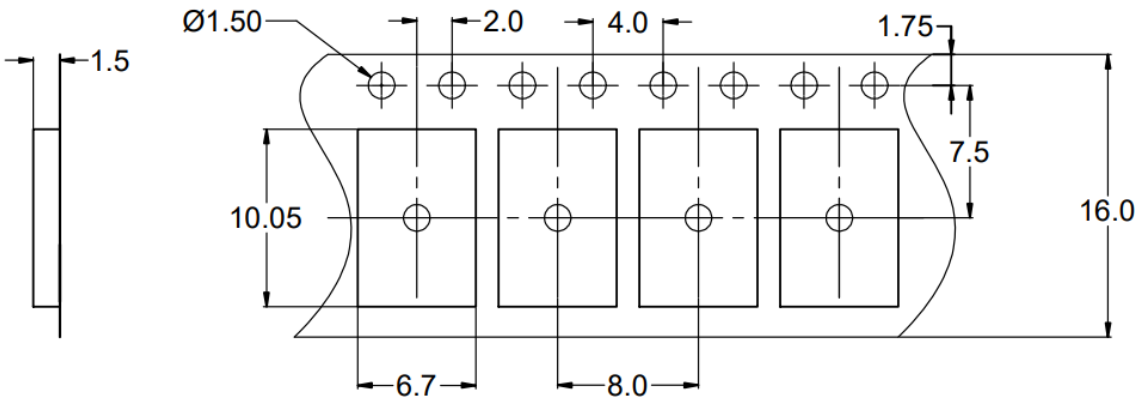


SOLDER PASTE EXAMPLE
BASED ON 0.125mm THICK STENCIL

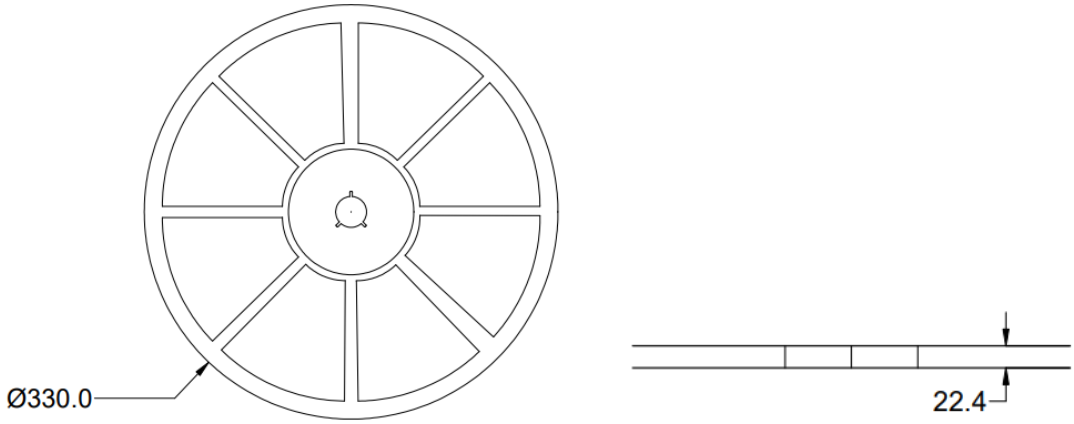


12 TAPE AND REEL INFORMATION

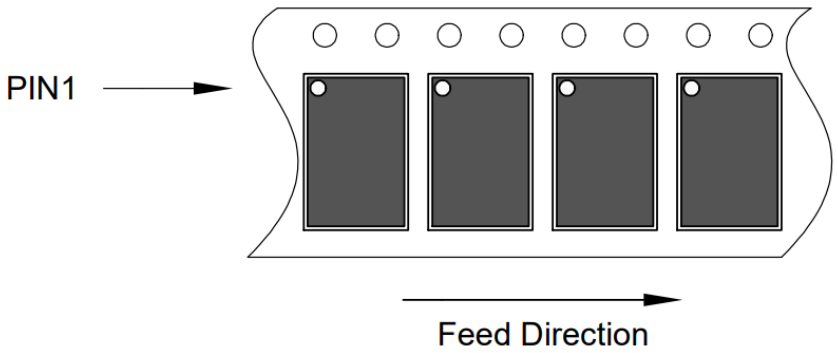
Tape Dimensions



Reel Dimensions



PIN1 Orientation in Tape



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