

Specification

RS2G32LV4D4BDT-46IT

Industrial LPDDR4/4X

200-ball FBGA

Revision History

| Rev | Date | Changes | Remark |
|------|------------|-----------------------------|-------------|
| V1.0 | 2022/12/08 | Basic spec and architecture | Preliminary |
| | | | |

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LPDDR4X/LPDDR4 SDRAM

RS2G32LV4D4BDT-46IT

Features

This data sheet is for LPDDR4X and LPDDR4 unified product based on LPDDR4X information. As for LPDDR4 setting, refer to General LPDDR4 Specification at the end of this datasheet.

- Ultra-low-voltage core and I/O power supplies
 - V_{DD1} = 1.70-1.95V; 1.80V nominal
 - V_{DD2} = 1.06-1.17V; 1.10V nominal
 - V_{DDQ} = 0.57-0.65V; 0.60V nominal
Or V_{DDQ} = 1.06-1.17V; 1.10V nominal
- Frequency range
 - 2133-10 MHz (data rate range per pin:4266-20 Mb/s)
- 16 *n* prefetch DDR architecture
- 8 internal banks per channel for concurrent operation
- Single-data-rate CMD / ADR entry
- Bidirectional / differential data strobe per byte lane
- Programmable READ and WRITE latencies (RL / WL)
- Programmable and on-the-fly burst lengths (BL = 16, 32)
- Directed per-bank refresh for concurrent bank operation and ease of command scheduling
- Up to 8.53 GB / s per die x16 channel
- On-chip temperature sensor to control self refresh rate
- Partial-array self refresh (PASR)
- Selectable output drive strength (DS)
- Clock-stop capability
- RoHS-compliant, “green” packaging
- Programmable V_{SS} (ODT) termination
- Single-ended CK and DQS support

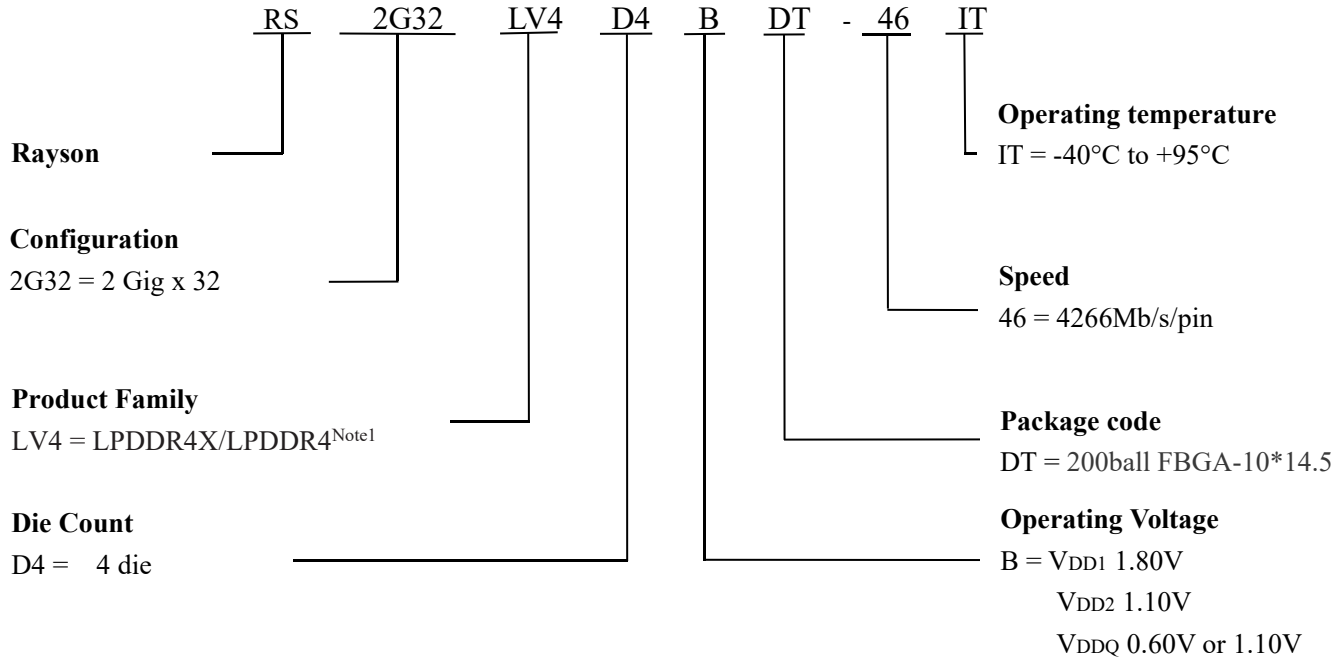
Options

- $V_{DD1}/V_{DD2}/V_{DDQ}$: 1.80V/1.10V/0.60V or 1.10V B
- Array configuration
 - 2 Gig x 32 2G32
 - (2 channels x 16 I/O*2ranks)
- Device configuration
 - 1G16 *4 die in package D4
- FBGA “green” package
 - 200-ball FBGA (10mm x14.5mm DT
 - Seated height: 1.1mm Max)
- Speed grade, cycle time
 - 468ps@ RL = 36/40 -46
- Operating temperature range
 - -40°C to + 95°C IT

Marking

Part Number Ordering Information

Figure 1: Part Number Chart



Note1: LPDDR4X: V_{DDQ}=0.60V; LPDDR4: V_{DDQ}=1.10V;

Table 1:Key Timing Parameters

| Speed Grade | Clock Rate (MHz) | Data Rate (Mb/s/pin) | WRITE Latency | | READ Latency | |
|-------------|------------------|----------------------|---------------|-------|--------------|-------------|
| | | | Set A | Set B | DBI Disabled | DBI Enabled |
| -46 | 2133 | 4266 | 18 | 34 | 36 | 40 |

Table 2: Part Number List

| Part Number | Total Density | Data Rate | Operating temperature |
|---------------------|---------------|---------------|-----------------------|
| RS2G32LV4D4BDT-46IT | 8GB(64Gb) | 4266 Mb/s/pin | -40°C to + 95°C |

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Product Specification

General Description

The 16Gb mobile low-power DDR4 SDRAM with low VDDQ (LPDDR4X) is a high-speed, CMOS dynamic random-access memory device. This 8-bank device is internally configured with $\times 16$ I/O.

General Notes

Throughout the data sheet, figures and text refer to DQs as DQ. DQ should be interpreted as any or all DQ collectively, unless stated otherwise.

DQS and CK should be interpreted as DQS_t, DQS_c and CK_t, CK_c respectively, unless stated otherwise. CA includes all CA pins used for a given density.

In timing diagrams, CMD is used as an indicator only. Actual signals occur on CA[5:0].

V_{REF} indicates V_{REFCA} and V_{REFDQ} .

Complete functionality may be described throughout the entire document. Any page or diagram may have been simplified to convey a topic and may not be inclusive of all requirements.

Any specific requirement takes precedence over a general statement.
Any functionality not specifically stated herein is considered undefined, illegal, not supported, and will result in unknown operation.

For single-ended CK and DQS features or specifications, refer to the LPDDR4X SingleEnded CK and DQS Addendum.

Device Configuration

Table 3: Device Configuration

| Device Configuration | | 2G32 (64Gb/package) |
|---------------------------------|-------------------|------------------------|
| Die Organization in the package | Channel A, rank 0 | x16 mode × 1 die |
| | Channel A, rank 1 | x16 mode × 1 die |
| | Channel B, rank 0 | x16 mode × 1 die |
| | Channel B, rank 1 | x16 mode × 1 die |
| Die addressing | Bank address | BA[2:0] |
| | Row address | R[16:0] |
| | Column address | C[9:0] |

Note: 1. Refer to Package Block Diagram section in Product Specification and SDRAM Addressing section in General LPDDR4X specification.

Refresh Requirement Parameters

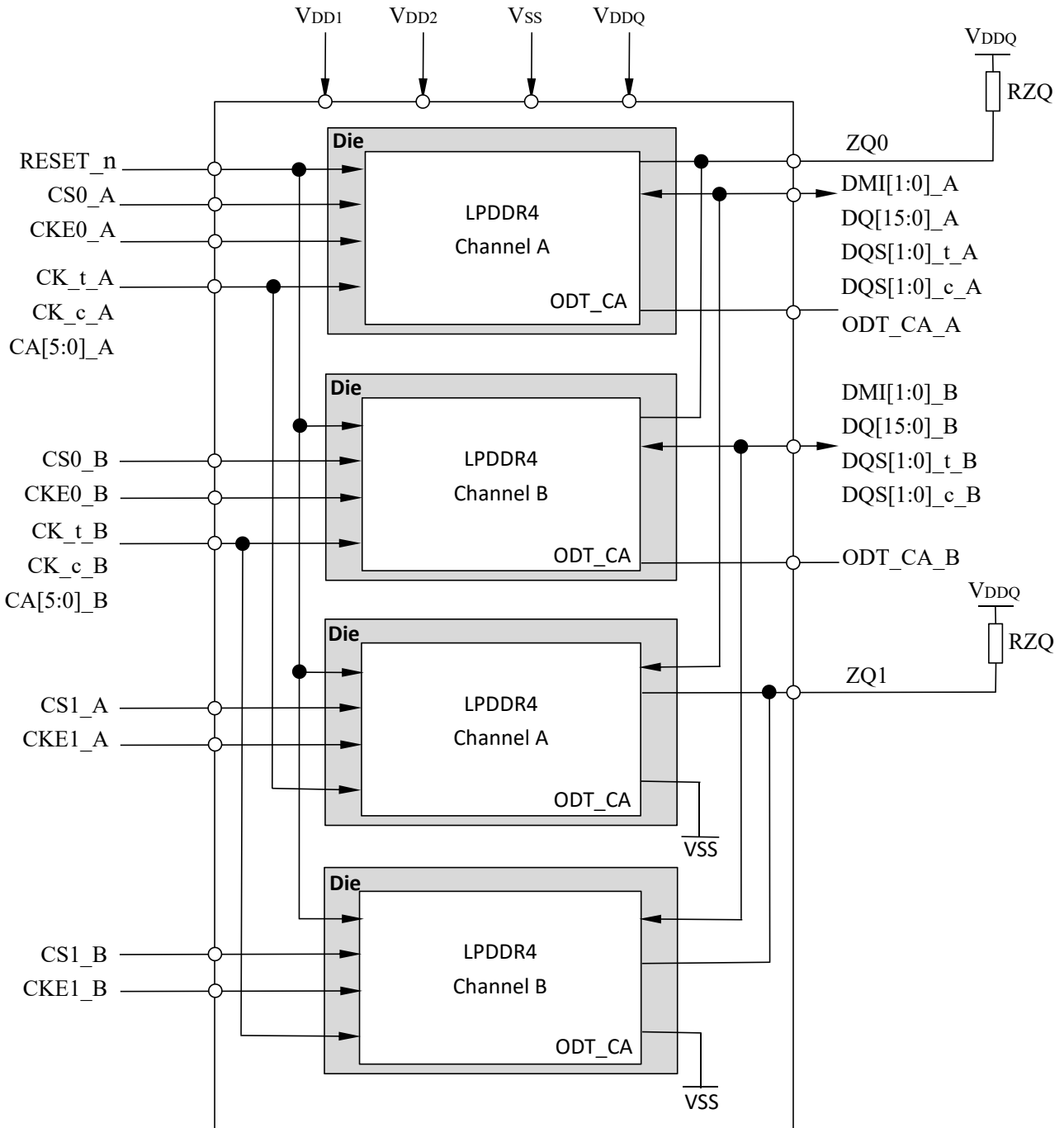
Table 4: Refresh Requirement Parameters

| Parameter | Symbol | 16Gb Single-Channel Die | unit |
|------------------------------------------------------------|----------------------|----------------------------|------|
| REFRESH cycle time (all banks) | ^t RFCab | 380 | ns |
| REFRESH cycle time (per bank) | ^t RFCpb | 190 | ns |
| Per bank refresh to per bank refresh time (different bank) | ^t PBR2PBR | 90 | ns |

Note: 1. This table only describes refresh parameters which are density dependent. Refer to Refresh Requirement section in General LPDDR4X specification for all the refresh parameters.

Package Block Diagrams

Figure 1: Quad-Die, Dual-Channel, Dual-Rank Package Block Diagram (x32 I/O)



Note:

1. ODT(ca) for rank 0 of each channel is wired to the respective ODT ball. ODT(ca) for rank 1 of each channel is wired to VSS in the package.

Ball Assignments and Descriptions Dual-Rank

Figure 2: 200-Ball Dual-Channel, Dual-Rank Discrete FBGA

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 |
|----|------------------|-----------------|------------------|------------------|------------------|---|---|------------------|------------------|------------------|-----------------|------------------|
| A | DNU | DNU | V _{SS} | V _{DD2} | ZQ0 | | | ZQ1 | V _{DD2} | V _{SS} | DNU | DNU |
| B | DNU | DQ0_A | V _{DDQ} | DQ7_A | V _{DDQ} | | | V _{DDQ} | DQ15_A | V _{DDQ} | DQ8_A | DNU |
| C | V _{SS} | DQ1_A | DMIO_A | DQ6_A | V _{SS} | | | V _{SS} | DQ14_A | DMI1_A | DQ9_A | V _{SS} |
| D | V _{DDQ} | V _{SS} | DQS0_t_A | V _{SS} | V _{DDQ} | | | V _{DDQ} | V _{SS} | DQS1_t_A | V _{SS} | V _{DDQ} |
| E | V _{SS} | DQ2_A | DQS0_c_A | DQ5_A | V _{SS} | | | V _{SS} | DQ13_A | DQS1_c_A | DQ10_A | V _{SS} |
| F | V _{DD1} | DQ3_A | V _{DDQ} | DQ4_A | V _{DD2} | | | V _{DD2} | DQ12_A | V _{DDQ} | DQ11_A | V _{DD1} |
| G | V _{SS} | ODT_CA_A | V _{SS} | V _{DD1} | V _{SS} | | | V _{SS} | V _{DD1} | V _{SS} | NC | V _{SS} |
| H | V _{DD2} | CA0_A | CS1_A | CS0_A | V _{DD2} | | | V _{DD2} | CA2_A | CA3_A | CA4_A | V _{DD2} |
| J | V _{SS} | CA1_A | V _{SS} | CKE0_A | CKE1_A | | | CK_t_A | CK_c_A | V _{SS} | CA5_A | V _{SS} |
| K | V _{DD2} | V _{SS} | V _{DD2} | V _{SS} | NC | | | NC | V _{SS} | V _{DD2} | V _{SS} | V _{DD2} |
| L | | | | | | | | | | | | |
| M | | | | | | | | | | | | |
| N | V _{DD2} | V _{SS} | V _{DD2} | V _{SS} | NC | | | NC | V _{SS} | V _{DD2} | V _{SS} | V _{DD2} |
| P | V _{SS} | CA1_B | V _{SS} | CKE0_B | CKE1_B | | | CK_t_B | CK_c_B | V _{SS} | CA5_B | V _{SS} |
| R | V _{DD2} | CA0_B | CS1_B | CS0_B | V _{DD2} | | | V _{DD2} | CA2_B | CA3_B | CA4_B | V _{DD2} |
| T | V _{SS} | ODT_CA_B | V _{SS} | V _{DD1} | V _{SS} | | | V _{SS} | V _{DD1} | V _{SS} | RESET_n | V _{SS} |
| U | V _{DD1} | DQ3_B | V _{DDQ} | DQ4_B | V _{DD2} | | | V _{DD2} | DQ12_B | V _{DDQ} | DQ11_B | V _{DD1} |
| V | V _{SS} | DQ2_B | DQS0_c_B | DQ5_B | V _{SS} | | | V _{SS} | DQ13_B | DQS1_c_B | DQ10_B | V _{SS} |
| W | V _{DDQ} | V _{SS} | DQS0_t_B | V _{SS} | V _{DDQ} | | | V _{DDQ} | V _{SS} | DQS1_t_B | V _{SS} | V _{DDQ} |
| Y | V _{SS} | DQ1_B | DMI0_B | DQ6_B | V _{SS} | | | V _{SS} | DQ14_B | DMI1_B | DQ9_B | V _{SS} |
| AA | DNU | DQ0_B | V _{DDQ} | DQ7_B | V _{DDQ} | | | V _{DDQ} | DQ15_B | V _{DDQ} | DQ8_B | DNU |
| AB | DNU | DNU | V _{SS} | V _{DD2} | V _{SS} | | | V _{SS} | V _{DD2} | V _{SS} | DNU | DNU |

Top View (ball down)

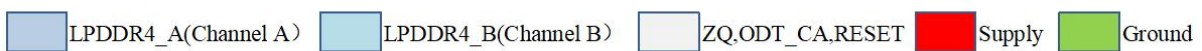
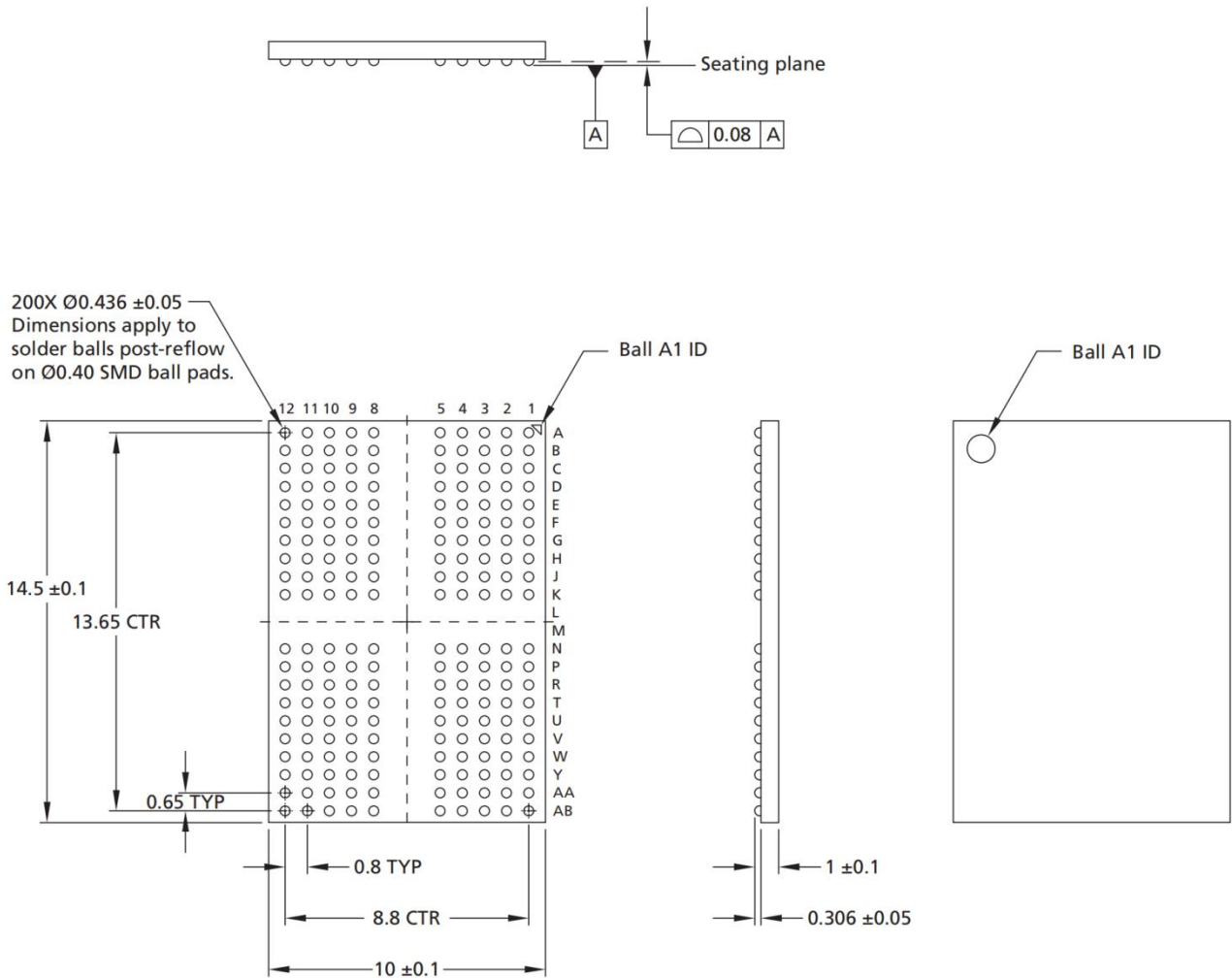


Table 5: Ball/Pad Descriptions

| Symbol | Type | Description |
|--------------------------------------------------------------|-----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CK_t_A, CK_c_A CK_t_B, CK_c_B | Input | Clock: CK_t and CK_c are differential clock inputs. All address, command and control input signals are sampled on positive edge of CK_t and the negative edge of CK_c. AC timings for CA parameters are referenced to clock. Each channel (A, B) has its own clock pair. |
| CKE0_A, CKE1_A CKE0_B, CKE1_B | Input | Clock enable: CKE HIGH activates and CKE LOW deactivates the internal clock signals, input buffers, and output drivers. Power-saving modes are entered and exited via CKE transitions. CKE is sampled at the rising edge of CK. |
| CS0_A, CS1_A CS0_B, CS1_B | Input | Chip select: Each channel (A, B) has its own CS signals. |
| CA[5:0]_A CA[5:0]_B | Input | Command/address inputs: Provide the command and address inputs according to the command truth table. Each channel (A, B) has its own CA signals. |
| ODT_CA_A ODT_CA_B | Input | LPDDR4X CA ODT Control: The ODT_CA pin is ignored by LPDDR4X devices. CA ODT is fully controlled through MR11 and MR22. The ODT_CA pin shall be connected to a valid logic level. |
| DQ[15:0]_A DQ[15:0]_B | I/O | Data input/output: Bidirectional data bus. |
| DQS[1:0]_t_A DQS[1:0]_c_A DQS[1:0]_t_B DQS[1:0]_c_B | I/O | Data strobe: DQS_t and DQS_c are bidirectional differential output clock signals used to strobe data during a READ or WRITE. The data strobe is generated by the DRAM for a READ and is edge-aligned with data. The data strobe is generated by the SoC memory controller for a WRITE and is trained to precede data. Each byte of data has a data strobe signal pair. Each channel (A, B) has its own DQS_t and DQS_c strobes. |
| DMI[1:0]_A DMI[1:0]_B | I/O | Data mask/Data bus inversion: DMI is a dual use bidirectional signal used to indicate data to be masked, and data which is inverted on the bus. For data bus inversion (DBI), the DMI signal is driven HIGH when the data on the data bus is inverted, or driven LOW when the data is in its normal state. DBI can be disabled via a mode register setting. For data mask, the DMI signal is used in combination with the data lines to indicate data to be masked in a MASK WRITE command (see the Data Mask (DM) and Data Bus Inversion (DBI) sections for details). The data mask function can be disabled via a mode register setting. Each byte of data has a DMI signal. Each channel has its own DMI signals. |
| ZQ0, ZQ1 | Reference | ZQ calibration reference: Used to calibrate the output drive strength and the termination resistance. The ZQ pin shall be connected to V _{DDQ} through a 240Ω ±1% resistor. |
| VDDQ, VDD1, VDD2 | Supply | Power supplies: Isolated on the die for improved noise immunity. |
| Vss | Supply | Ground reference: Power supply ground reference. |
| RESET_n | Input | RESET: When asserted LOW, the RESET pin resets all channels of the die. |
| DNU | – | Do not use: Must be grounded or left floating. |
| NC | – | No connect: Not internally connected. |

Package Dimensions

Figure 3: 200-Ball TFBGA – 10mm x 14.5mm x 1.1mm (Package Code: DT)



Notes: 1. All dimensions are in millimeters.

MR0, MR3, MR[6:5], MR8, MR13, MR[25:24] Definition

Table 6: Mode Register Contents

Notes 1 and 2 apply to entire table.

| Mode Register | OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 | |
|---------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|------------------------------------------|-------|---------------|-------------------|--------------|-------|--|
| MR0 | | | Single-ended mode | | | RFM support | Latency mode | REF | |
| | OP[0] = 1b: Only modified refresh mode supported OP[1] = 0b: Device supports normal latency OP[2] = 0b: Device supports TRR OP[5] = 1b: Device supports single-ended mode | | | | | | | | |
| MR3 | | | | | | PPRP ³ | | | |
| | OP[2] = 0b: PPR protection disabled (default); 1b: PPR protection enabled; | | | | | | | | |
| MR5 | Manufacturer ID | | | | | | | | |
| | 1111 1111b : Micron | | | | | | | | |
| MR6 | Revision ID1 | | | | | | | | |
| | 0000 0111b | | | | | | | | |
| MR8 | I/O width | | Density | | | | | | |
| | OP[7:6] = 00b: x16/channel | | OP[5:2] = 0110b: 16Gb single-channel die | | | | | | |
| MR13 | | | | | | VRO | | | |
| | OP[2] = 0b: Normal operation (default); 1b: Output the V _{REF(CA)} value on DQ7 and V _{REF(DQ)} value on DQ6 | | | | | | | | |
| MR24 | TRR mode | | | | Unlimited MAC | MAC value | | | |
| | OP[3:0] = 1000b: Unlimited MAC; OP[7] = 0b: Disable (default); 1b: Reserved; | | | | | | | | |
| MR25 | PPR resources ⁴ | | | | | | | | |
| | Bank7 | Bank6 | Bank5 | Bank4 | Bank3 | Bank2 | Bank1 | Bank0 | |
| | 0b: PPR resource is not available; 1b: PPR resource is available | | | | | | | | |

Notes:

1. The contents of Product Specific Mode Register definition will reflect information specific to each die in these packages.
2. Other bits not defined above and other mode registers are referred to Mode Register Assignments and Definitions section.
3. When not using PPR function, PPR protection should be enabled to prevent unintended PPR entry. (MR3 OP[2] = 1b).
4. Before using PPR function, confirm the availability of PPR resource by reading MR25.

LPDDR4X I_{DD} Parameters

Refer to I_{DD} Specification Parameters and Test Conditions section for detailed conditions.

Table 7-1: LPDDR4X I_{DD} Parameters – Single Die

$V_{DD2} = 1.06\text{--}1.17\text{V}$; $V_{DDQ} = 0.57\text{--}0.65\text{V}$; $V_{DD1} = 1.70\text{--}1.95\text{V}$;

| Symbol | Supply | Speed Grade | Unit | Note |
|---------------------|------------------|-------------|------|------|
| | | 4266 Mb/s | | |
| I _{DD01} | V _{DD1} | 5.00 | mA | |
| I _{DD02} | V _{DD2} | 26.00 | | |
| I _{DD0Q} | V _{DDQ} | 0.75 | | |
| I _{DD2P1} | V _{DD1} | 2.40 | mA | |
| I _{DD2P2} | V _{DD2} | 3.40 | | |
| I _{DD2PQ} | V _{DDQ} | 0.75 | | |
| I _{DD2PS1} | V _{DD1} | 2.40 | mA | |
| I _{DD2PS2} | V _{DD2} | 3.40 | | |
| I _{DD2PSQ} | V _{DDQ} | 0.75 | | |
| I _{DD2N1} | V _{DD1} | 2.40 | mA | |
| I _{DD2N2} | V _{DD2} | 14.00 | | |
| I _{DD2NQ} | V _{DDQ} | 0.75 | | |
| I _{DD2NS1} | V _{DD1} | 2.40 | mA | |
| I _{DD2NS2} | V _{DD2} | 12.00 | | |
| I _{DD2NSQ} | V _{DDQ} | 0.75 | | |
| I _{DD3P1} | V _{DD1} | 2.40 | mA | |
| I _{DD3P2} | V _{DD2} | 6.20 | | |
| I _{DD3PQ} | V _{DDQ} | 0.75 | | |
| I _{DD3PS1} | V _{DD1} | 2.40 | mA | |
| I _{DD3PS2} | V _{DD2} | 6.20 | | |
| I _{DD3PSQ} | V _{DDQ} | 0.75 | | |
| I _{DD3N1} | V _{DD1} | 3.40 | mA | |
| I _{DD3N2} | V _{DD2} | 16.00 | | |
| I _{DD3NQ} | V _{DDQ} | 0.75 | | |
| I _{DD3NS1} | V _{DD1} | 3.40 | mA | |
| I _{DD3NS2} | V _{DD2} | 14.00 | | |
| I _{DD3NSQ} | V _{DDQ} | 0.75 | | |

Table 7-2: LPDDR4X I_{DD} Parameters – Single Die (Continued)

$V_{DD2} = 1.06\text{--}1.17\text{V}$; $V_{DDQ} = 0.57\text{--}0.65\text{V}$; $V_{DD1} = 1.70\text{--}1.95\text{V}$;

| Symbol | Supply | Speed Grade | Unit | Note |
|---------|------------------|-------------|------|------|
| | | 4266 Mb/s | | |
| IDD4R1 | V _{DD1} | 11.00 | mA | 2,3 |
| IDD4R2 | V _{DD2} | 205.00 | | |
| IDD4RQ | V _{DDQ} | 63.00 | | |
| IDD4W1 | V _{DD1} | 11.00 | mA | 2 |
| IDD4W2 | V _{DD2} | 160.00 | | |
| IDD4WQ | V _{DDQ} | 0.75 | | |
| IDD51 | V _{DD1} | 23.00 | mA | |
| IDD52 | V _{DD2} | 110.00 | | |
| IDD5Q | V _{DDQ} | 0.75 | | |
| IDD5AB1 | V _{DD1} | 6.60 | mA | |
| IDD5AB2 | V _{DD2} | 24.00 | | |
| IDD5ABQ | V _{DDQ} | 0.75 | | |
| IDD5PB1 | V _{DD1} | 4.80 | mA | |
| IDD5PB2 | V _{DD2} | 24.00 | | |
| IDD5PBQ | V _{DDQ} | 0.75 | | |

Notes:

1. Published I_{DD} values except I_{DD4RQ} are the maximum I_{DD} values considering the worst-case conditions of process, temperature, and voltage.
2. BL = 16, DBI disabled.
3. I_{DD4RQ} value is reference only. Typical value. $V_{OH} = 0.5 \times V_{DDQ}$; $T_C = 25^\circ\text{C}$.

Table 8: IDD6 Full-Array Self Refresh Current – Single Die

$V_{DD2} = 1.06\text{--}1.17\text{V}$; $V_{DDQ} = 0.57\text{--}0.65\text{V}$; $V_{DD1} = 1.70\text{--}1.95\text{V}$;

| Temperature | Supply | Full-Array Self | Unit |
|-------------|------------------|-----------------|------|
| 25°C | V _{DD1} | 0.52 | mA |
| | V _{DD2} | 1.16 | |
| | V _{DDQ} | 0.01 | |
| 95°C | V _{DD1} | 4.30 | mA |
| | V _{DD2} | 9.00 | |
| | V _{DDQ} | 0.75 | |

Notes:

- IDD6 25°C is the typical value in the distribution with nominal V_{DD} and a reference-only value. IDD6 95°C is the maximum IDD guaranteed value considering the worst-case conditions of process, temperature, and voltage.*