

Rockchip RK3036G Datasheet

**Revision 1.0
Sep. 2017**

Revision History

Date	Revision	Description
2017-9-1	1.1	Update the feature error
2017-05-19	1.0	Initial Release

Rockchip Confidential

Table of Content

Table of Content	3
Figure Index	5
Table Index 6	
Warranty Disclaimer.....	7
Chapter 1 Introduction	8
1.1 Overview.....	8
1.2 Features.....	8
1.2.1 Microprocessor	8
1.2.2 Memory Organization	8
1.2.3 Internal Memory.....	8
1.2.4 External Memory or Storage device	9
1.2.5 System Component.....	9
1.2.6 Video CODEC	11
1.2.7 HEVC Decoder.....	11
1.2.8 JPEG CODEC	11
1.2.9 Image Enhancement	11
1.2.10 Graphics Engine	12
1.2.11 Video OUT	12
1.2.12 Audio Interface.....	13
1.2.13 Connectivity.....	14
1.2.14 Others	15
1.3 Block Diagram	15
Chapter 2 Package information	17
2.1 Ordering information	17
2.2 Top Marking.....	17
2.3 Dimension	17
2.4 Pin Number Order	19
2.5 Power/ground IO descriptions	23
2.6 Function IO description	25
2.7 IO pin name descriptions.....	35
2.8 IO Type.....	37
Chapter 3 Electrical Specification	39
3.1 Absolute Maximum Ratings.....	39
3.2 Recommended Operating Conditions.....	39
3.3 Recommended Operating Frequency	40
3.4 Electrical Characteristics for General IO.....	41
3.5 Electrical Characteristics for PLL	41
3.6 Electrical Characteristics for USB Interface	41
3.7 Electrical Characteristics for DDR IO	42

3.8 Electrical Characteristics for eFuse..... 42

3.9 Electrical Characteristics for HDMI 42

3.10 Electrical Characteristics for VDAC 43

Chapter 4 Thermal Management 44

4.1 Overview..... 44

4.2 Package Thermal Characteristics 44

Rockchip Confidential

Figure Index

Fig. 1-1 RK3036G Block Diagram	16
Fig. 2-2 RK3036G BGA236 Package Top View.....	17
Fig. 2-3 RK3036G BGA236 Package Bottom View	18
Fig. 2-4 RK3036G BGA236 Package Side View	18
Fig. 2-5 RK3036G BGA236 Package Side View	18
Fig. 2-7 RK3036G BGA236 Package Dimension	19

Rockchip Confidential

Table Index

Table 2-2 RK3036G BGA236 Number Order Information	19
Table 2-4 RK3036G Power/Ground IO information for BGA236	23
Table 2-5 RK3036G IO List	25
Table 2-6 RK3036G IO function description list.....	35
Table 2-7 RK3036G IO Type List.....	37
Table 3-1 RK3036G absolute maximum ratings	39
Table 3-2 RK3036G recommended operating conditions	39
Table 3-3 RK3036G DC Characteristics.....	40
Table 3-4 Recommended operating frequency for PD_BUS domain	40
Table 3-5 RK3036G Electrical Characteristics for Digital General IO	41
Table 3-6 RK3036G Electrical Characteristics for PLL	41
Table 3-7 RK3036G Electrical Characteristics for USB Interface.....	41
Table 3-8 RK3036G Electrical Characteristics for DDR IO	42
Table 3-9 RK3036G Electrical Characteristics for eFuse.....	42
Table 3-10 RK3036G Electrical Characteristics for HDMI	42
Table 3-11 RK3036G Electrical Characteristics for VDAC	43
Table 4-1 RK3036G Thermal Resistance Characteristics	44

Warranty Disclaimer

Rockchip Electronics Co., Ltd makes no warranty, representation or guarantee (expressed, implied, statutory, or otherwise) by or with respect to anything in this document, and shall not be liable for any implied warranties of non-infringement, merchantability or fitness for a particular purpose or for any indirect, special or consequential damages.

Information furnished is believed to be accurate and reliable. However, Rockchip Electronics Co., Ltd assumes no responsibility for the consequences of use of such information or for any infringement of patents or other rights of third parties that may result from its use.

Rockchip Electronics Co., Ltd's products are not designed, intended, or authorized for using as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Rockchip Electronics Co., Ltd's product could create a situation where personal injury or death may occur, should buyer purchase or use Rockchip Electronics Co., Ltd's products for any such unintended or unauthorized application, buyers shall indemnify and hold Rockchip Electronics Co.,Ltd and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, expenses, and reasonable attorney fees arising out of, either directly or indirectly, any claim of personal injury or death that may be associated with such unintended or unauthorized use, even if such claim alleges that Rockchip Electronics Co.,Ltd was negligent regarding the design or manufacture of the part.

Copyright and Patent Right

Information in this document is provided solely to enable system and software implementers to use Rockchip Electronics Co.,Ltd 's products. There are no expressed or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Rockchip Electronics Co., Ltd does not convey any license under its patent rights nor the rights of others.

All copyright and patent rights referenced in this document belong to their respective owners and shall be subject to corresponding copyright and patent licensing requirements.

Trademarks

Rockchip and Rockchip™ logo and the name of Rockchip Electronics Co., Ltd's products are trademarks of Rockchip Electronics Co.,Ltd. and are exclusively owned by Rockchip Electronics Co.,Ltd. References to other companies and their products use trademarks owned by the respective companies and are for reference purpose only.

Confidentiality

The information contained herein (including any attachments) is confidential. The recipient hereby acknowledges the confidentiality of this document, and except for the specific purpose, this document shall not be disclosed to any third party.

Reverse engineering or disassembly is prohibited.

ROCKCHIP ELECTRONICS CO.,LTD. RESERVES THE RIGHT TO MAKE CHANGES IN ITS PRODUCTS OR PRODUCT SPECIFICATIONS WITH THE INTENT TO IMPROVE FUNCTION OR DESIGN AT ANY TIME AND WITHOUT NOTICE AND IS NOT REQUIRED TO UNDATE THIS DOCUMENTATION TO REFLECT SUCH CHANGES.

Copyright © 2017 Rockchip Electronics Co., Ltd.

All rights reserved. No part of this publication may be reproduced, stored in a retrieval system, or transmitted in any form or by any means, electric or mechanical, by photocopying, recording, or otherwise, without the prior written consent of Rockchip Electronics Co., Ltd.

Chapter 1 Introduction

1.1 Overview

RK3036G is a low power, high performance processor solution for OTT TV BOX, and other digital multimedia applications, and integrates dual-core Cortex-A7, with separate NEON coprocessor and 128KB L2 Cache.

Many embedded powerful hardware engines provide optimized performance for high-end application. RK3036G supports almost full-format 1080P H.264 decoder and H.265 decoder, high-quality JPEG decoder and special image preprocessor and postprocessor.

Embedded 3D GPU makes RK3036G completely compatible with OpenGL ES1.1 and 2.0, OpenVG1.1 etc.

RK3036G has high-performance external memory interface (DDR3/DDR3L) capable of sustaining demanding memory bandwidths, also provides a complete set of peripheral interface to support very flexible applications.

1.2 Features

The features listed below which may or may not be present in actual product, may be subject to the third party licensing requirements. Please contact Rockchip for actual product feature configurations and licensing requirements.

1.2.1 Microprocessor

- Dual-core ARM Cortex-A7 MPCore processor, a high-performance, low-power and cached application processor.
- Full implementation of the ARM architecture v7-A instruction set, ARM Neon Advanced SIMD (single instruction, multiple data) support for accelerated media and signal processing computation.
- Superscalar, variable length, out-of-order pipeline with dynamic branch prediction, 8-stage pipeline.
- Include VFPv3 hardware to support single and double-precision add, subtract, divide, multiply and accumulate, and square root operations.
- SCU ensures memory coherency between the two CPUs.
- Integrated 32KB L1 instruction cache, 32KB L1 data cache with 4-way set associative
- 128KByte unified L2 Cache.

1.2.2 Memory Organization

- Internal on-chip memory
 - 16KB BootRom
 - 8KB internal SRAM
- External off-chip memory[®]
 - DDR3-1066/DDR3L-1066, 16bits data width, 2 ranks, totally 2GB(max) address space, maximum address space for one rank is 1GB.
 - Asynchronous Nand Flash(include LBA Nand), 8bits data width, 1 bank, 60bits ECC.

1.2.3 Internal Memory

- Internal BootRom
 - Size : 16KB
 - Support system boot from the following device:
 - ◆ 8bits Asynchronous Nand Flash
 - ◆ SPI Nand Flash
 - ◆ SPI Nor Flash
 - ◆ eMMC card
 - ◆ SD card
 - Support system code download by the following interface:

- ◆ USB OTG interface
 - Support secure boot.
- Internal SRAM
 - Size : 8KB

1.2.4 External Memory or Storage device

- Dynamic Memory Interface (DDR3/DDR3L)
 - Compatible with JEDEC standard DDR3/DDR3L SDRAM
 - Data rates up to 1066Mbps(533MHz) for DDR3/DDR3L
 - Support up to 2 ranks (chip selects), maximum 1GB address space per rank
 - data width is 8bbits or 16bits, software programmable
 - Four host ports with 64bits/128bits AXI bus interface for system access, AXI bus clock is asynchronous with DDR clock
 - Programmable timing parameters to support DDR3/DDR3L SDRAM from various vendor
 - Advanced command reordering and scheduling to maximize bus utilization
 - Low power modes, such as power-down and self-refresh for DDR3 /DDR3L SDRAM
 - Programmable output and ODT impedance with dynamic PVT compensation
 - Support one low-power work mode: power down DDR PHY and most of DDR IO except two cs and cke output signals, make SDRAM still in self-refresh state to prevent data missing
- Nand Flash Interface
 - Support asynchronous nand flash, each channel 8bits, 1 bank
 - Support configurable interface timing
 - Embedded special DMA interface to do data transfer
 - Also support data transfer together with PERI_DMAC in SoC system
- eMMC Interface
 - Compatible with standard eMMC interface
 - Support MMC4.5 protocol
 - Provide eMMC boot sequence to receive boot data from external eMMC device
 - Support CRC generation and error detection
 - Embedded clock adjusting for high speed transfer
 - Support block size from 1 to 65535Bytes
 - Support 8bits data width with signal data rate or dual data rate
- SD/MMC Interface
 - Compatible with SD2.0, MMC4.5
 - Support FIFO over-run and under-run prevention by stopping card clock automatically
 - Support CRC generation and error detection
 - Embedded clock adjusting for high speed transfer
 - Support block size from 1 to 65535Bytes
 - Support 4bits data width signal data rate or dual data rate
- Serial Flash Controller(SFC)
 - One on-chip SFC inside RK3036G
 - Support command/address/data x1/x2/x4 bits mode configurable
 - Support 2 chip select
 - Support connected to serial nor flash or serial nand flash

1.2.5 System Component

- CRU (clock & reset unit)
 - Support clock gating control for individual components inside RK3036G
 - One oscillator with 24MHz clock input and three embedded PLLs: ARM PLL, DDR

- PLL, GENERAL PLL
- Support global soft-reset control for whole SOC, also individual soft-reset for every components
- Timer
 - Four on-chip 64bits Timers in SOC with interrupt-based operation
 - Provide two operation modes: free-running and user-defined count
 - Support timer work state checkable
 - 24MHz or pclk_peri for clock input selectable
- PWM
 - Four on-chip PWMs with interrupt-based operation
 - Programmable pre-scaled operation to bus clock and then further scaled
 - Embedded 32-bit timer/counter facility
 - Support capture mode
 - Support continuous mode or one-shot mode
 - Provides reference mode and output various duty-cycle waveform
- WatchDog
 - 32 bits watchdog counter width
 - Counter clock is from APB bus clock
 - Counter counts down from a preset value to 0 to indicate the occurrence of a timeout
 - WDT can perform two types of operations when timeout occurs:
 - ◆ Generate a system reset
 - ◆ First generate an interrupt and if this is not cleared by the service routine by the time a second timeout occurs then generate a system reset
 - Programmable reset pulse length
 - Totally 16 defined-ranges of main timeout period
- Bus Architecture
 - 128bit/64-bit/32-bit multi-layer AXI/AHB/APB composite bus architecture
 - Five embedded AXI interconnect:
 - ◆ BUS interconnect
 - ◆ PERI interconnect
 - ◆ Display interconnect
 - ◆ GPU interconnect
 - ◆ VCODEC interconnect
 - For each interconnect with AXI/AHB/APB composite bus, clocks for AXI/AHB/APB domains are always synchronous, and different integer ratio is supported for them.
 - Flexible different QoS solution to improve the utility of bus bandwidth
- Interrupt Controller
 - Support 3 PPI interrupt source and 128 SPI interrupt sources input from different components inside RK3036G
 - Support 16 software-triggered interrupts
 - Input interrupt level is fixed, only high-level sensitive
 - Two interrupt outputs (nFIQ and nIRQ) separately for each Cortex-A7, both are low-level sensitive
 - Support different interrupt priority for each interrupt source, and they are always software-programmable
- DMAC
 - Micro-code programming based DMA
 - The specific instruction set provides flexibility for programming DMA transfers
 - Linked list DMA function is supported to complete scatter-gather transfer
 - Support internal instruction cache

- Embedded DMA manager thread
- Support data transfer types with memory-to-memory, memory-to-peripheral, peripheral-to-memory
- Signals the occurrence of various DMA events using the interrupt output signals
- Mapping relationship between each channel and different interrupt outputs is software-programmable
- One embedded DMA controller, PERI_DMACH is for peripheral system
- PERI_DMACH features:
 - ◆ 8 channels totally
 - ◆ 13 hardware request from peripherals
 - ◆ 2 interrupt output

1.2.6 Video CODEC

- Embedded memory management unit(MMU)
- Video Decoder
 - Real-time video decoder of MPEG-1, MPEG-2, MPEG-4,H.263, H.264, VP8, MVC
 - Error detection and concealment support for all video formats
 - Output data format is YUV420 semi-planar, and YUV400(monochrome) is also supported for H.264
 - H.264 up to HP level 5.2 : 1080p@30fps (1920x1088)[®]
 - MPEG-4 up to ASP level 5 : 1080p@30fps (1920x1088)
 - MPEG-2 up to MP : 1080p@30fps (1920x1088)
 - MPEG-1 up to MP : 1080p@30fps (1920x1088)
 - H.263 : 576p@30fps (720x576)
 - VP8 : 1080p@30fps (1920x1088)
 - MVC : 1080p@30fps (1920x1088)
 - For H.264, image cropping not supported
 - For MPEG-4,GMC(global motion compensation)not supported
 - For MPEG-4 SP/H.263, using a modified H.264 in-loop filter to implement deblocking filter in post-processor unit

1.2.7 HEVC Decoder

- HEVC/H.265 decoder according to Main specification
- Support up to 1920x1088 (1080P@30fps) resolution
- Embedded memory management unit(MMU)
- Stream error detector (28 IDs)
- Internal 128k cache for bandwidth reduction
- Multi-clock domains and auto clock-gating design for power saving

1.2.8 JPEG CODEC

- JPEG decoder
 - Input JPEG file : YCbCr 4:0:0, 4:2:0, 4:2:2, 4:4:0, 4:1:1 and 4:4:4 sampling formats
 - Output raw image : YCbCr 4:0:0, 4:2:0, 4:2:2, 4:4:0, 4:1:1 and 4:4:4 semi-planar
 - Decoder size is from 48x48 to 8176x8176(66.8Mpixels)
 - Support JPEG ROI(region of image) decode
 - Maximum data rate[®] is up to 76million pixels per second
 - Embedded memory management unit(MMU)

1.2.9 Image Enhancement

- Image Post-Processor(embedded inside video decoder)
 - Combined with HD video decoder and JPEG decoder, post-processor can read input data directly from decoder output to reduce bus bandwidth
 - Also work as a stand-alone mode, its input data is from image data stored in external memory

- Input data format:
 - ◆ Any format generated by video decoder in combined mode
 - ◆ YCbCr4:2:0 semi-planar
 - ◆ YCbCr4:2:0 planar
 - ◆ YCbYCr 4:2:2
 - ◆ YCrYCb 4:2:2
 - ◆ CbYCrY 4:2:2
 - ◆ CrYCbY 4:2:2
- Output data format:
 - ◆ YCbCr4:2:0 semi-planar
 - ◆ YCbYCr 4:2:2
 - ◆ YCrYCb 4:2:2
 - ◆ CbYCrY 4:2:2
 - ◆ CrYCbY 4:2:2
 - ◆ Fully configurable ARGB channel lengths and locations inside 32bits, such as ARGB8888, RGB565, ARGB4444 etc.
- Input image size:
 - ◆ Combined mode: from 48x48 to 8176x8176 (66.8Mpixels)
 - ◆ Stand-alone mode: width from 48 to 8176, height from 48 to 8176, and maximum size limited to 16.7Mpixels
 - ◆ Step size is 16 pixels
- Output image size: from 16x16 to 1920x1088 (horizontal step size 8, vertical step size 2)
- Support image up-scaling:
 - ◆ Bicubic polynomial interpolation with a four-tap horizontal kernel and a two-tap vertical kernel
 - ◆ Arbitrary non-integer scaling ratio separately for both dimensions
 - ◆ Maximum output width is 3x input width
 - ◆ Maximum output height is 3x input height
- Support image down-scaling:
 - ◆ Arbitrary non-integer scaling ratio separately for both dimensions
 - ◆ Unlimited down-scaling ratio
- Support YUV to RGB color conversion, compatible with BT.601-5, BT.709 and user definable conversion coefficient
- Support dithering (Allegro dither algorithm) for 4/5/6bit RGB channel precision
- Support RGB image contrast/brightness/color saturation adjustment
- Support image cropping & digital zoom only for JPEG or stand-alone mode
- Support picture in picture
- Support image rotation (horizontal flip, vertical flip, rotation 90,180 or 270 degrees)

1.2.10 Graphics Engine

- 3D Graphics Engine(GPU)
 - High performance OpenGL ES1.1 and 2.0, OpenVG1.1 etc.
 - Embedded 1 shader core with shared hierarchical tiler
 - Separate vertex(geometry) and fragment(pixel) processing for maximum parallel throughput
 - Provide MMU and L2 Cache with 64KB size

1.2.11 Video OUT

- Display Interface
 - Display process
 - ◆ Background layer
 - programmable 24-bit color
 - ◆ Win0 (Video) layer
 - RGB888, ARGB888, RGB565, YCbCr422, YCbCr420, YCbCr444

- Support virtual display
 - 1/8 to 8 scaling-down and scaling-up engine
 - ✧ Scale up using bicubic or bilinear
 - ✧ Scale down using bilinear
 - ✧ 1 Bicubic table: catrom
 - ✧ coord 8bit, coe 8bit signed
 - ◆ Win1 (UI) layer:
 - RGB888, ARGB888, RGB565
 - Support virtual display
 - ◆ Hardware cursor:
 - 8bpp
 - Support two sizes: 32x32,64x64
 - ◆ Overlay:
 - Win0/Win1 256 level alpha blending(support pre-multiplied alpha)
 - Win0/Win1 overlay position exchangeable
 - Win0/Win1 Transparency color key
 - Win0/Win1 global/per-pixel alpha
 - HWC 256 level alpha blending
 - HWC global/per-pixel alpha
 - Others
 - ◆ Max output resolution: 1920x1080
 - ◆ Max scanning timing: 4096x4096
 - ◆ YcbCr2RGB(rec601-mpeg/rec601-jpeg/rec709)and RGB2YcbCr
 - ◆ Support BCSH function
 - ◆ QoS request signals
 - ◆ Bus address alignment
 - ◆ Embedded memory management unit(MMU)
- HDMI TX
 - HDMI version 1.4a, HDCP revision 1.2 and DVI version 1.0 compliant transmitter
 - Supports DTV from 480i to 1080i/p HD resolution
 - Supports data rate from 25MHz, 1.65bps up to 3.4Gbps over a Single channel HDMI
 - TMDS Tx Drivers with programmable output swing, resister values and pre-emphasis
 - Digital video interface supports a pixel size of 24, 30, 36, 48bits color depth in RGB
 - S/PDIF output supports PCM and compressed audio transmission using IEC60958 and IEC61937
 - Multiphase 4MHz fixed bandwidth PLL with low jitter
 - HDCP encryption and decryption engine contains all the necessary logic to encrypt the incoming audio and video data
 - Support HDMI LipSync if needed
 - Lower power operation with optimal power management feature
 - The EDID and CEC function are also supported
 - Optional Monitor Detection supported through Hot Plug
 - Support 8-channel I2S and 8-channel SPDIF input
- CVBS output
 - 10-bit Resolution
 - PAL/NTSC encoding
 - Programmable luma filter coefficient
 - Programmable luma/chroma delay
 - Programmable brightness/contrast

1.2.12 Audio Interface

- I2S/PCM with 8ch
 - Up to 8 channels (4xTX, 1xRX)

- Audio resolution from 16bits to 32bits
- Sample rate up to 192KHz
- Provides master and slave work mode, software configurable
- Support 3 I2S formats (normal, left-justified, right-justified)
- Support 4 PCM formats(early, late1, late2, late3)
- I2S and PCM mode cannot be used at the same time
- SPDIF
 - Support 8 channels audio stream
 - Support two 16-bit audio data store together in one 32-bit wide location
 - Support biphasic format stereo audio data output
 - Support 16 to 31 bit audio data left or right justified in 32-bit wide sample data buffer
 - Support 16, 20, 24 bits audio data transfer in linear PCM mode
 - Support non-linear PCM transfer
- Audio CODEC
 - 24bit DAC with 95dB SNR
 - Support Line-out
 - Support Mono, Stereo, 5.1 HiFi channel performance
 - Integrated digital interpolation and decimation filter.
 - Sampling rate of 8kHz/12kHz/16kHz/24kHz/32kHz/44.1kHz/48kHz/96kHz
 - Optional fractional PLL available that support 6MHz to 20MHz clock input to any clock

1.2.13 Connectivity

- SDIO interface
 - Embedded one SDIO interface
 - Compatible with SDIO 3.0 protocol
 - 4bits data bus width
- EMAC 10/100M Ethernet Controller
 - IEEE802.3u compliant Ethernet Media Access Controller(MAC)
 - Support only RMII(Reduced MII) mode
 - 10Mbps and 100Mbps compatible
 - Automatic retry and automatic collision frame deletion
 - Full duplex support with flow-control
 - Address filtering(broadcast, multicast, logical, physical)
- SPI Controller
 - One on-chip SPI controller inside RK3036G
 - Support serial-master and serial-slave mode, software-configurable
 - DMA-based or interrupt-based operation
 - Embedded two 32x16bits FIFO for TX and RX operation respectively
 - Support 2 chip-selects output in serial-master mode
- UART Controller
 - Three on-chip UART controllers inside RK3036G
 - DMA-based or interrupt-based operation
 - For all UART, two 64Bytes FIFOs are embedded for TX/RX operation respectively
 - Support 5bit,6bit,7bit,8bit serial data transmit or receive
 - Standard asynchronous communication bits such as start, stop and parity
 - Support different input clock for UART operation to get up to 4Mbps or other special baud rate
 - Support non-integer clock divides for baud clock generation
- I2C controller

- Three on-chip I2C controllers in RK3036G
- Multi-master I2C operation
- Support 7bits and 10bits address mode
- Software programmable clock frequency and transfer rate up to 400Kbit/s in the fast mode
- Serial 8bits oriented and bidirectional data transfers can be made at up to 100Kbit/s in the standard mode
- GPIO
 - All of GPIOs can be used to generate interrupt to Cortex-A7
 - The pull direction(pullup or pulldown) for all of GPIOs are software-programmable
 - All of GPIOs are always in input direction in default after power-on-reset
 - The drive strength is not software-programmable, determined by the GPIO type; except special GPIOs for HDMI iomux
- USB Host2.0
 - Compatible with USB Host2.0 specification
 - Supports high-speed(480Mbps), full-speed(12Mbps) and low-speed(1.5Mbps) mode
 - Provides 16 host mode channels
 - Support periodic out channel in host mode
- USB OTG2.0
 - Compatible with USB OTG2.0 specification
 - Supports high-speed(480Mbps), full-speed(12Mbps) and low-speed(1.5Mbps) mode
 - Support up to 9 device mode endpoints in addition to control endpoint 0
 - Support up to 6 device mode IN endpoints including control endpoint 0
 - Endpoints 1/3/5/7 can be used only as data IN endpoint
 - Endpoints 2/4/6 can be used only as data OUT endpoint
 - Endpoints 8/9 can be used as data OUT and IN endpoint
 - Provides 9 host mode channels

1.2.14 Others

- eFuse
 - One 256bits high-density electrical Fuse, organized as 32x8bits
 - Program 1-bit each time in program mode
 - Read 8-bit each time in read mode
 - Three operation modes: program mode, read mode, inactive mode
- Package Type
 - eLQFP176(body: 20mm x 20mm; pin pitch: 0.4mm)
 - BGA236(body: 12mm x 12mm; pin pitch: 0.65mm)

Notes:

- ①: DDR3/DDR3L are not used simultaneously
- ②: In RK3036G, Video decoder and HEVC are not used simultaneously
- ③: Actual maximum frame rate will depend on the clock frequency and system bus performance
- ④: Actual maximum data rate will depend on the clock frequency and JPEG compression rate

1.3 Block Diagram

The following diagram shows the basic block diagram for RK3036G.

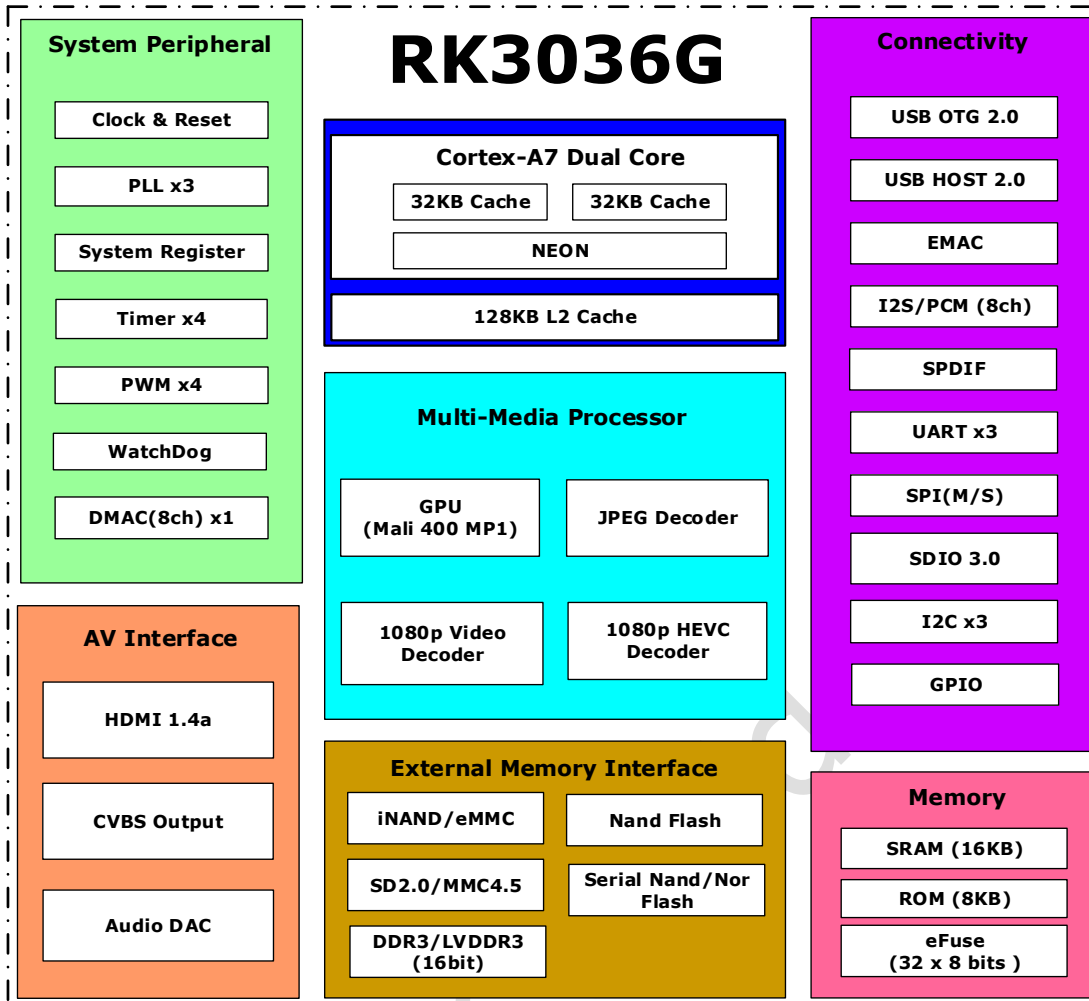


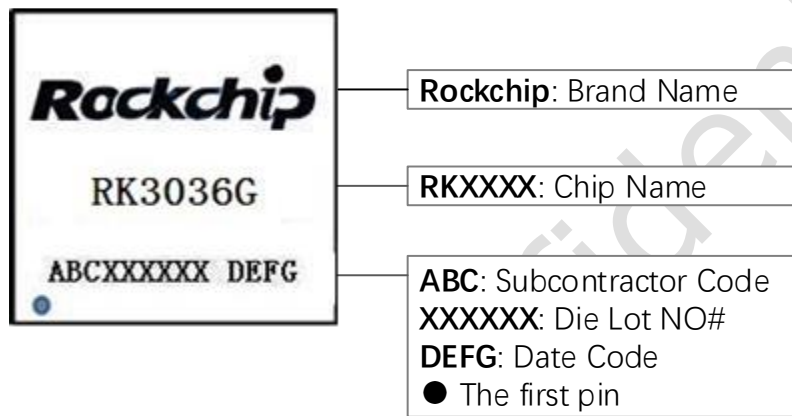
Fig. 1-1 RK3036G Block Diagram

Chapter 2 Package information

2.1 Ordering information

Orderable Device	RoHS status	Package	Package Qty	Device Feature
RK3036G	RoHS	TFBGA236	1890	Dual Core AP

2.2 Top Marking



2.3 Dimension

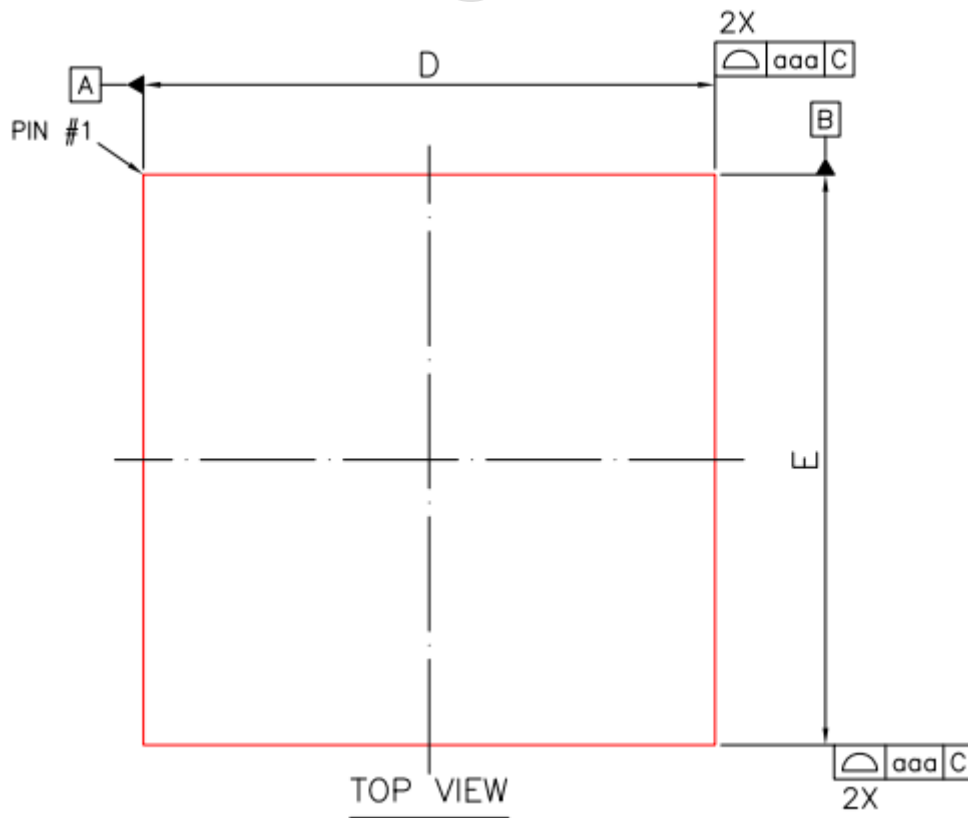


Fig. 2-1 RK3036G BGA236 Package Top View

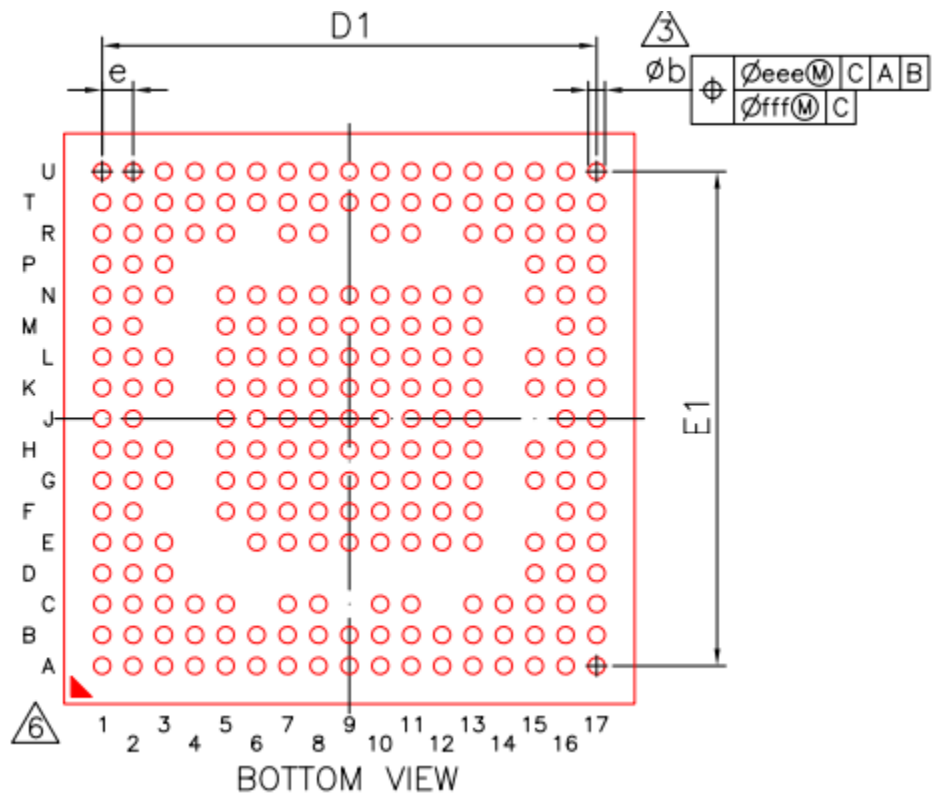


Fig. 2-2 RK3036G BGA236 Package Bottom View

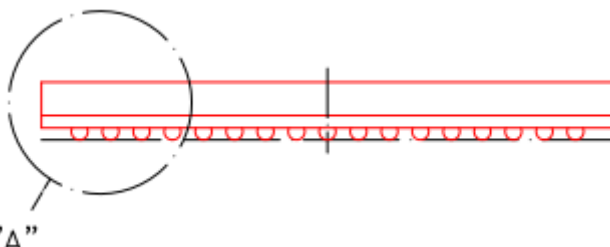


Fig. 2-3 RK3036G BGA236 Package Side View

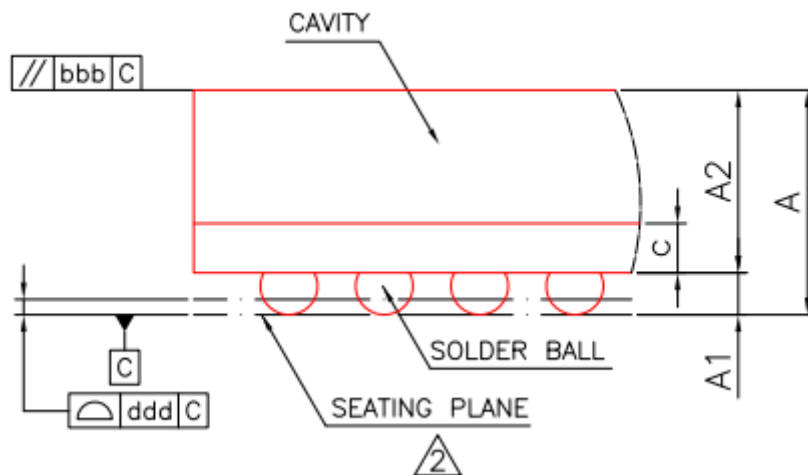


Fig. 2-4 RK3036G BGA236 Package Side View

Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.14	1.21	1.28	0.045	0.048	0.050
A1	0.20	0.25	0.30	0.008	0.010	0.012
A2	0.91	0.96	1.01	0.036	0.038	0.040
c	0.22	0.26	0.30	0.009	0.010	0.012
D	11.90	12.00	12.10	0.469	0.472	0.476
E	11.90	12.00	12.10	0.469	0.472	0.476
D1	----	10.40	----	----	0.409	----
E1	----	10.40	----	----	0.409	----
e	----	0.65	----	----	0.026	----
b	0.30	0.35	0.40	0.012	0.014	0.016
aaa		0.15			0.006	
bbb		0.10			0.004	
ddd		0.10			0.004	
eee		0.15			0.006	
fff		0.08			0.003	
MD/ME	17/17					

Fig. 2-5 RK3036G BGA236 Package Dimension

2.4 Pin Number Order

Table 2-1 RK3036G BGA236 Number Order Information

Pin Index	Pin Name	Pin Index	Pin Name
C13	DDR_DQ0	N2	GPIO2_A7
B12	DDR_DQ1	M2	GPIO2_B0
A15	DDR_DQ2	L3	GPIO2_B1
A11	DDR_DQ3	N1	GPIO2_B3
A13	DDR_DQ4	E16	GPIO0_D2
C11	DDR_DQ5	E17	GPIO0_D3/IR
B13	DDR_DQ6	T14	GPIO0_C4/DRIVE_VBUS
A12	DDR_DQ7	A17	GPIO0_C2/UART0_RTSN
E3	DDR_DQ8	A16	GPIO0_C3/UART0_CTSN
G1	DDR_DQ9	B15	GPIO0_C0/UART0_TX
D1	DDR_DQ10	C14	GPIO0_C1/UART0_RX
H1	DDR_DQ11	P1	GPIO2_C6/UART1_RX
F1	DDR_DQ12	P2	GPIO2_C7/UART1_TX
G2	DDR_DQ13	U17	GPIO1_D0/FLASH_D0/EMMC_D0/SFC_SIO 0
F2	DDR_DQ14	P15	GPIO1_D1/FLASH_D1/EMMC_D1/SFC_SIO 1

Pin Index	Pin Name	Pin Index	Pin Name
G3	DDR_DQ15	T17	GPIO1_D2/FLASH_D2/EMMC_D2/SFC_SIO 2
A14	DDR_DQS0	R16	GPIO1_D3/FLASH_D3/EMMC_D3/SFC_SIO 3
B14	DDR_DQS0_N	R17	GPIO1_D4/FLASH_D4/EMMC_D4/SPI_RXD
E1	DDR_DQS1	N15	GPIO1_D5/FLASH_D5/EMMC_D5/SPI_TXD
E2	DDR_DQS1_N	P16	GPIO1_D6/FLASH_D6/EMMC_D6/SPI_CSN 0
B11	DDR_DM0	P17	GPIO1_D7/FLASH_D7/EMMC_D7/SPI_CSN 1
H2	DDR_DM1	N16	GPIO2_A0/FLASH_ALE/SPI_CLK
A1	DDR_A0	N17	GPIO2_A1/FLASH_CLE/EMMC_CLK
C8	DDR_A1	M16	GPIO2_A2/FLASH_WRN/SFC_CSN0
B2	DDR_A2	M17	GPIO2_A3/FLASH_RDN/SFC_CSN1
A2	DDR_A3	L15	GPIO2_A4/FLASH_RDY/EMMC_CMD/SFC_C LK
B8	DDR_A4	L16	GPIO2_A6/FLASH_CS0
C3	DDR_A5	H17	GPIO1_B7/SDMMC0_CMD
A10	DDR_A6	H16	GPIO1_C0/SDMMC0_CLKO
C1	DDR_A7	J17	GPIO1_C1/SDMMC0_DET
C10	DDR_A8	J16	GPIO1_C2/SDMMC0_D0/UART2_RX
B1	DDR_A9	K17	GPIO1_C3/SDMMC0_D1/UART2_TX
A7	DDR_A10	K16	GPIO1_C4/SDMMC0_D2/JTAG_TCK
A9	DDR_A11	K15	GPIO1_C5/SDMMC0_D3/JTAG_TMS
A8	DDR_A12	G15	GPIO0_B0/SDMMC1_CMD/I2S1_SDO
C2	DDR_A13	F16	GPIO0_B1/SDMMC1_CLKO/I2S1_MCLK
B10	DDR_A14	F17	GPIO0_B3/SDMMC1_D0/I2S1_LRCK_RX
B9	DDR_A15	G16	GPIO0_B4/SDMMC1_D1/I2S1_LRCK_TX
B5	DDR_CLK_N	G17	GPIO0_B5/SDMMC1_D2/I2S1_SDI
A5	DDR_CLK	H15	GPIO0_B6/SDMMC1_D3/I2S1_SCLK
B7	DDR_BA0	D17	GPIO1_A0/I2S_MCLK
C7	DDR_BA1	C17	GPIO1_A1/I2S_SCLK
B3	DDR_BA2	E15	GPIO1_A2/I2S_LRCK_RX/PWM0
A6	DDR_ODT0	D16	GPIO1_A3/I2S_LRCK_TX
D2	DDR_ODT1	D15	GPIO1_A5/I2S_SDI

Pin Index	Pin Name	Pin Index	Pin Name
C5	DDR_CSN0	B17	GPIO1_A4/I2S_SDO0
B4	DDR_CSN1	C16	GPIO2_D6/I2S_SDO1
B6	DDR_CKE	C15	GPIO2_D5/I2S_SDO2
A4	DDR_RASN	B16	GPIO2_D4/I2S_SDO3
A3	DDR_CASN	K5	VCCIO1
C4	DDR_WEN	N10	VCCIO2
D3	DDR_RESETN	K13	VCCIO3
H5	DDR_VDD1	H13	VCCIO4
G5	DDR_VDD2	J5	CVDD1
F5	DDR_VDD3	L5	CVDD2
E6	DDR_VDD4	N11	CVDD3
E7	DDR_VDD5	N12	CVDD4
E8	DDR_VDD6	M13	CVDD5
L17	NPOR	L13	CVDD6
M1	TEST	G13	CVDD7
L2	XOUT24M	E13	CVDD8
L1	XIN24M	E9	CVDD9
K1	DPLL_DVDD11	H3	VSS1
K2	APLL_DVDD11	E10	VSS2
J2	PLL_VCCIO	E11	VSS3
T2	USB1_DP	E12	VSS4
T1	USB1_DM	F6	VSS5
U2	USB0_ID	F7	VSS6
U1	USB_EXTR	F8	VSS7
R3	USB0_VBUS	F9	VSS8
U3	USB0_DM	F10	VSS9
T3	USB0_DP	F11	VSS10
N5	USB_DVDD11	F12	VSS11
M5	USB_AVDD33	F13	VSS12
K3	EFUSE	G6	VSS13

Pin Index	Pin Name	Pin Index	Pin Name
U4	HDMI_TX3N	G7	VSS14
T4	HDMI_TX3P	G8	VSS15
U5	HDMI_TX0N	G9	VSS16
T5	HDMI_TX0P	G10	VSS17
U6	HDMI_TX1N	G11	VSS18
T6	HDMI_TX1P	G12	VSS19
U7	HDMI_TX2N	H6	VSS20
T7	HDMI_TX2P	H7	VSS21
R4	HDMI_EXTR	H8	VSS22
N3	GPIO1_B0/HDMI_CEC	H9	VSS23
P3	GPIO1_B3/HDMI_HPD	H10	VSS24
R1	GPIO1_B2/HDMI_SCL	H11	VSS25
R2	GPIO1_B1/HDMI_SDA	H12	VSS26
N6	HDMI_AVDD33	J6	VSS27
R5	HDMI_DVDD1V1_1	J7	VSS28
R7	HDMI_DVDD1V1_2	J8	VSS29
T8	VDAC_IOUTP	J9	VSS30
R8	VDAC_IOUTN	J10	VSS31
N9	VDAC_IREF	J11	VSS32
N7	VDAC_AVDD	J12	VSS33
N8	VDAC_AGND	J13	VSS34
U9	CODEC_AOL	K6	VSS35
T10	CODEC_AOR	K7	VSS36
U10	CODEC_VCM	K8	VSS37
U8	CODEC_AVDD	K9	VSS38
T9	CODEC_AVSS	K10	VSS39
U11	GPIO2_C3/MAC_TXD0	K11	VSS40
T11	GPIO2_C2/MAC_TXD1	K12	VSS41
R10	GPIO2_C1/MAC_RXD0	L6	VSS42
T12	GPIO2_C0/MAC_RXD1	L7	VSS43

Pin Index	Pin Name	Pin Index	Pin Name
U12	GPIO2_D1/MAC_MDC	L8	VSS44
U13	GPIO2_B7/MAC_RXER	L9	VSS45
R11	GPIO2_B6/MAC_CLK_IN/MAC_CLK_OUT	L10	VSS46
R13	GPIO2_B5/MAC_TXEN	L11	VSS47
T13	GPIO2_B4/MAC_MDIO	L12	VSS48
U14	GPIO2_B2/MAC_CRCS	M6	VSS49
T15	GPIO0_A1/PWM2/I2C0_SDA	M7	VSS50
U15	GPIO0_A0/PWM1/I2C0_SCL	M8	VSS51
R14	GPIO0_A2/I2C1_SCL	M9	VSS52
R15	GPIO0_A3/I2C1_SDA	M10	VSS53
U16	GPIO2_C4/I2C2_SDA	M11	VSS54
T16	GPIO2_C5/I2C2_SCL	M12	VSS55
N13	GPIO0_D4/SPDIF	J1	VSS56

2.5 Power/ground IO descriptions

Table 2-2 RK3036G Power/Ground IO information for BGA236

Group	Pin# (BGA236)	Descriptions
GND	H3,E10,E11,E12,F6,F7,F8,F9,F10,F11,F12,F13,G6,G7,G8,G9,G10,G11,G12,H6,H7,H8,H9,H10,H11,H12,J6,J7,J8,J9,J10,J11,J12,J13,K6,K7,K8,K9,K10,K11,K12,L6,L7,L8,L9,L10,L11,L12,M6,M7,M8,M9,M10,M11,M12,J1	Internal Core Ground, Digital IO Ground, Analog IO Ground
CVDD	L5,N11,N12,M13,L13,G13,E13,E9	Internal Core Power Digital GPIO Power
VCCIO	K5,N10,K13,H13	GPIO Power
DDR_VDD	H5,G5,F5,E6,E7,E8	DDR3 Digital IO Power
APLL_DVDD11	K2	ARM PLL Analog Power
DPLL_DVDD11	K1	DDR PLL Analog Power
PLL_VCCIO	J2	PLL Power
USB_DVDD11	N5	USB OTG2.0/Host2.0 Digital Power
USB_AVDD33	M5	USB OTG2.0/Host2.0 Analog Power
CODEC_AVDD	U8	Audio Codec Analog Power
CODEC_AVSS	T9	Audio Codec Analog Ground
HDMI_AVDD33	N6	HDMI Power

Group	Pin# (BGA236)	Descriptions
HDMI_DVDD1V1_1	R5	HDMI Power
HDMI_DVDD1V1_2	R7	HDMI Power
VDAC_AGND	N8	Video DAC Analog Ground
VDAC_AVDD	N7	Video DAC Analog Power

2.6 Function IO description

Table 2-3 RK3036G IO List

PIN	Pin Name	Pad type	IO Pull	Default function	Defual function description	Function 2	Function 3
Part A							
C13	DDR_DQ0	A		DDR_DQ0	DRAM0 data port		
B12	DDR_DQ1	A		DDR_DQ1	DRAM0 data port		
A15	DDR_DQ2	A		DDR_DQ2	DRAM0 data port		
A11	DDR_DQ3	A		DDR_DQ3	DRAM0 data port		
A13	DDR_DQ4	A		DDR_DQ4	DRAM0 data port		
C11	DDR_DQ5	A		DDR_DQ5	DRAM0 data port		
B13	DDR_DQ6	A		DDR_DQ6	DRAM0 data port		
A12	DDR_DQ7	A		DDR_DQ7	DRAM0 data port		
E3	DDR_DQ8	A		DDR_DQ8	DRAM0 data port		
G1	DDR_DQ9	A		DDR_DQ9	DRAM0 data port		
D1	DDR_DQ10	A		DDR_DQ10	DRAM0 data port		
H1	DDR_DQ11	A		DDR_DQ11	DRAM0 data port		
F1	DDR_DQ12	A		DDR_DQ12	DRAM0 data port		
G2	DDR_DQ13	A		DDR_DQ13	DRAM0 data port		
F2	DDR_DQ14	A		DDR_DQ14	DRAM0 data port		
G3	DDR_DQ15	A		DDR_DQ15	DRAM0 data port		
A14	DDR_DQS0	A		DDR_DQS0	DRAM0 data strobe 0		
B14	DDR_DQS0_N	A		DDR_DQS0_N	DRAM0 data strobe 0		
E1	DDR_DQS1	A		DDR_DQS1	DRAM0 data strobe 1		
E2	DDR_DQS1_N	A		DDR_DQS1_N	DRAM0 data strobe 1		
B11	DDR_DM0	A		DDR_DM0	DRAM0 data mask 0		
H2	DDR_DM1	A		DDR_DM1	DRAM0 data mask 1		
A1	DDR_A0	A		DDR_A0	DRAM0 address port		
C8	DDR_A1	A		DDR_A1	DRAM0 address port		
B2	DDR_A2	A		DDR_A2	DRAM0 address port		

PIN	Pin Name	Pad type	IO Pull	Default function	Defual function description	Function 2	Function 3
A2	DDR_A3	A		DDR_A3	DRAM0 address port		
B8	DDR_A4	A		DDR_A4	DRAM0 address port		
C3	DDR_A5	A		DDR_A5	DRAM0 address port		
A10	DDR_A6	A		DDR_A6	DRAM0 address port		
C1	DDR_A7	A		DDR_A7	DRAM0 address port		
C10	DDR_A8	A		DDR_A8	DRAM0 address port		
B1	DDR_A9	A		DDR_A9	DRAM0 address port		
A7	DDR_A10	A		DDR_A10	DRAM0 address port		
A9	DDR_A11	A		DDR_A11	DRAM0 address port		
A8	DDR_A12	A		DDR_A12	DRAM0 address port		
C2	DDR_A13	A		DDR_A13	DRAM0 address port		
B10	DDR_A14	A		DDR_A14	DRAM0 address port		
B9	DDR_A15	A		DDR_A15	DRAM0 address port		
B5	DDR_CLK_N	A		DDR_CLK_N	DRAM0 differential clock output		
A5	DDR_CLK	A		DDR_CLK	DRAM0 differential clock output		
B7	DDR_BA0	A		DDR_BA0	DRAM0 bank select 0		
C7	DDR_BA1	A		DDR_BA1	DRAM0 bank select 1		
B3	DDR_BA2	A		DDR_BA2	DRAM0 bank select 2		
A6	DDR_ODT0	A		DDR_ODT0	DRAM0 on die termination control 0		
D2	DDR_ODT1	A		DDR_ODT1	DRAM0 on die termination control 1		
C5	DDR_CSN0	A		DDR_CSN0	DRAM0 chip select 0		
B4	DDR_CSN1	A		DDR_CSN1	DRAM0 chip select 1		
B6	DDR_CKE	A		DDR_CKE	DRAM0 clock enable		
A4	DDR_RASN	A		DDR_RASN	DRAM0 row address strobe output		
A3	DDR_CASN	A		DDR_CASN	DRAM0 column address strobe output		
C4	DDR_WEN	A		DDR_WEN	DRAM0 write enable strobe output		
D3	DDR_RESETN	A		DDR_RESETN	DRAM0 reset output		
H5	DDR_VDD1	AP		DDR_VDD1	DDR PHY power supply		

PIN	Pin Name	Pad type	IO Pull	Default function	Defual function description	Function 2	Function 3
G5	DDR_VDD2	AP		DDR_VDD2	DDR PHY power supply		
F5	DDR_VDD3	AP		DDR_VDD3	DDR PHY power supply		
E6	DDR_VDD4	AP		DDR_VDD4	DDR PHY power supply		
E7	DDR_VDD5	AP		DDR_VDD5	DDR PHY power supply		
E8	DDR_VDD6	AP		DDR_VDD6	DDR PHY power supply		
Part B							
L17	NPOR	I	up	NPOR	System reset input		
M1	TEST	I	down	TEST	Enter into test mode,default connect to VSS		
L2	XOUT24M	O		XOUT24M	Oscillator 24MHz clock output		
L1	XIN24M	I		XIN24M	Oscillator 24MHz clock input		
K1	DPLL_DVDD11	AP		DPLL_DVDD11	DPLL analog power supply		
K2	APLL_DVDD11	AP		APLL_DVDD11	APLL analog power supply		
J2	PLL_VCCIO	AP		PLL_VCCIO	PLL power		
T2	USB1_DP	A		USB1_DP	USB1 Data Plus port		
T1	USB1_DM	A		USB1_DM	USB1 Data Minus port		
U2	USB0_ID	A		USB0_ID	USB0 ID detect input,need external pull-up		
U1	USB_EXTR	A		USB_EXTR	USB0 130 Ω Reference external resistance		
R3	USB0_VBUS	A		USB0_VBUS	USB connected detect input		
U3	USB0_DM	A		USB0_DM	USB0 Data Minus port		
T3	USB0_DP	A		USB0_DP	USB0 Data Plus port		
N5	USB_DVDD11	AP		USB_DVDD11	USB 1.1V analog core supply		
M5	USB_AVDD33	AP		USB_AVDD33	USB 3.3V analog positive supply		
K3	EFUSE	AP		EFUSE	EFUSE VQPS Power supply		
Part C							
U4	HDMI_TX3N	A		HDMI_TX3N	HDMI differential pixel clock negative		
T4	HDMI_TX3P	A		HDMI_TX3P	HDMI differential pixel clock positive		
U5	HDMI_TX0N	A		HDMI_TX0N	HDMI channel 0 differential serial data negative		
T5	HDMI_TX0P	A		HDMI_TX0P	HDMI channel 0 differential serial data positive		

PIN	Pin Name	Pad type	IO Pull	Default function	Defual function description	Function 2	Function 3
U6	HDMI_TX1N	A		HDMI_TX1N	HDMI channel 1 differential serial data negative		
T6	HDMI_TX1P	A		HDMI_TX1P	HDMI channel 1 differential serial data positive		
U7	HDMI_TX2N	A		HDMI_TX2N	HDMI channel 2 differential serial data negative		
T7	HDMI_TX2P	A		HDMI_TX2P	HDMI channel 2 differential serial data positive		
R4	HDMI_EXTR	A		HDMI_EXTR	HDMI reference current generate,connect a 2K %1 resistor to VSS.		
N3	GPIO1_B0/HDMI_CEC	I/O	up	HDMI_CEC	HDMI CEC communication		
P3	GPIO1_B3/HDMI_HPD	I/O	down	HDMI_HPD	HDMI Hot Plug Detection input		
R1	GPIO1_B2/HDMI_SCL	I/O	up	HDMI_SCL	HDMI I2C serial port,need external pull-up		
R2	GPIO1_B1/HDMI_SDA	I/O	up	HDMI_SDA	HDMI I2C serial port,need external pull-up		
N6	HDMI_AVDD33	AP		HDMI_AVDD33	HDMI power supply		
R5	HDMI_DVDD1V1_1	AP		HDMI_DVDD1V1_1	HDMI power supply		
R7	HDMI_DVDD1V1_2	AP		HDMI_DVDD1V1_2	HDMI power supply		
Part D							
T8	VDAC_IOUTP	A		VDAC_IOUTP	Positive Output for DAC		
R8	VDAC_IOUTN	A		VDAC_IOUTN	Negative Output for DAC		
N9	VDAC_IREF	A		VDAC_IREF	VDAC reference current generate,connect a 1K13%1 % resistor to VSS.		
N7	VDAC_AVDD	AP		VDAC_AVDD	VDAC power supply		
N8	VDAC_AGND	AG		VDAC_AGND	VDAC GND		
Part E							
U9	CODEC_AOL	A		CODEC_AOL	Left channel output		
T10	CODEC_AOR	A		CODEC_AOR	Right channel output		
U10	CODEC_VCM	A		CODEC_VCM	CODEC VCM,connect 4.7uF capacitance to VSS		
U8	CODEC_AVDD	AP		CODEC_AVDD	CODEC POWER		
T9	CODEC_AVSS	AG		CODEC_AVSS	CODEC VSS		
Part F							
U11	GPIO2_C3/MAC_TXD0	I/O	down	MAC_TXD0	MAC transmit data		
T11	GPIO2_C2/MAC_TXD1	I/O	down	MAC_TXD1	MAC transmit data		

PIN	Pin Name	Pad type	IO Pull	Default function	Defual function description	Function 2	Function 3
R10	GPIO2_C1/MAC_RXD0	I/O	down	MAC_RXD0	MAC receive data		
T12	GPIO2_C0/MAC_RXD1	I/O	down	MAC_RXD1	MAC receive data		
U12	GPIO2_D1/MAC_MDC	I/O	down	MAC_MDC	MAC_Management clock		
U13	GPIO2_B7/MAC_RXER	I/O	down	MAC_RXER	MAC receive error		
R11	GPIO2_B6/MAC_CLK_IN/MAC_CLK_OUT	I/O	down	MAC_CLK_IN	MAC reference clock input	MAC_CLK_OUT	
R13	GPIO2_B5/MAC_TXEN	I/O	down	MAC_TXEN	MAC transmit enable		
T13	GPIO2_B4/MAC_MDIO	I/O	down	MAC_MDIO	MAC_Management command and data		
U14	GPIO2_B2/MAC_CRS	I/O	down	MAC_CRS	MAC carrier sense detect		
T15	GPIO0_A1/PWM2/I2C0_SDA	I/O	up	PWM2	CPU POWER dynamic voltage scaing control	I2C0_SDA	
U15	GPIO0_A0/PWM1/I2C0_SCL	I/O	up	BT_HOST_WAKE	BT module wake up CPU	I2C0_SCL	
R14	GPIO0_A2/I2C1_SCL	I/O	up	I2C1_SCL	I2C serial port 1,need external pull-up		
R15	GPIO0_A3/I2C1_SDA	I/O	up	I2C1_SDA	I2C serial port 1,need external pull-up		
U16	GPIO2_C4/I2C2_SDA	I/O	up	WIFI_HOST_WAKE	WIFI module wake up CPU		
T16	GPIO2_C5/I2C2_SCL	I/O	up	BT_WAKE	CPU wake up BT module		
N13	GPIO0_D4/SPDIF	I/O	down	SPDIF	SPDIF TX		
N2	GPIO2_A7	I/O	down	MUTE_CTL	AUDIO out mute control		
M2	GPIO2_B0	I/O	up	RECOVER	Low level into Recover		
L3	GPIO2_B1	I/O	down	STANDBY_LED	STANDBY LED control		
N1	GPIO2_B3	I/O	down				
E16	GPIO0_D2	I/O	down	OTG_DRV	USB OTG power control output		
E17	GPIO0_D3/IR	I/O	down	IR	IR receive input		
T14	GPIO0_C4/DRIVE_VBUS	I/O	down	HOST_VBUS	USB HOST power control output		
A17	GPIO0_C2/UART0_RTSN	I/O	up	UART0_RTSN	UART0 serial port, for BT module		
A16	GPIO0_C3/UART0_CTSN	I/O	up	UART0_CTSN	UART0 serial port, for BT module		
B15	GPIO0_C0/UART0_TX	I/O	down	UART0_TX	UART0 serial port, for BT module		
C14	GPIO0_C1/UART0_RX	I/O	up	UART0_RX	UART0 serial port, for BT module		
P1	GPIO2_C6/UART1_RX	I/O	up	LAN_RST	Ethernet reset output		
P2	GPIO2_C7/UART1_TX	I/O	down				

PIN	Pin Name	Pad type	IO Pull	Default function	Defual function description	Function 2	Function 3
Part G							
U17	GPIO1_D0/FLASH_D0/EMMC_D0/SFC_SIO0	I/O	up	FLASH_D0	Nand Flash/EMMC data port	EMMC_D0	SFC_SIO0
P15	GPIO1_D1/FLASH_D1/EMMC_D1/SFC_SIO1	I/O	up	FLASH_D1	Nand Flash/EMMC data port	EMMC_D1	SFC_SIO1
T17	GPIO1_D2/FLASH_D2/EMMC_D2/SFC_SIO2	I/O	up	FLASH_D2	Nand Flash/EMMC data port	EMMC_D2	SFC_SIO2
R16	GPIO1_D3/FLASH_D3/EMMC_D3/SFC_SIO3	I/O	up	FLASH_D3	Nand Flash/EMMC data port	EMMC_D3	SFC_SIO3
R17	GPIO1_D4/FLASH_D4/EMMC_D4/SPI_RXD	I/O	up	FLASH_D4	Nand Flash/EMMC data port	EMMC_D4	SPI_RXD
N15	GPIO1_D5/FLASH_D5/EMMC_D5/SPI_TXD	I/O	up	FLASH_D5	Nand Flash/EMMC data port	EMMC_D5	SPI_TXD
P16	GPIO1_D6/FLASH_D6/EMMC_D6/SPI_CSN0	I/O	up	FLASH_D6	Nand Flash/EMMC data port	EMMC_D6	SPI_CSN0
P17	GPIO1_D7/FLASH_D7/EMMC_D7/SPI_CSN1	I/O	up	FLASH_D7	Nand Flash/EMMC data port	EMMC_D7	SPI_CSN1
N16	GPIO2_A0/FLASH_ALE/SPI_CLK	I/O	down	FLASH_ALE	Nand flash address latch enable		SPI_CLK
N17	GPIO2_A1/FLASH_CLE/EMMC_CLK	I/O	down	FLASH_CLE	Nand flash command latch enable	EMMC_CLK	
M16	GPIO2_A2/FLASH_WRN/SFC_CSN0	I/O	up	FLASH_WRN	Nand flash write enable		SFC_CSN0
M17	GPIO2_A3/FLASH_RDN/SFC_CSN1	I/O	up	FLASH_RDN	Nand flash read enable		SFC_CSN1
L15	GPIO2_A4/FLASH_RDY/EMMC_CMD/SFC_CLK	I/O	up	FLASH_RDY	Nand flash read/busy output	EMMC_CMD	SFC_CLK
L16	GPIO2_A6/FLASH_CS0	I/O	up	FLASH_CS0	Nand flash select0 port		
Part H							
H17	GPIO1_B7/SDMMC0_CMD	I/O	up	SDMMC0_CMD	SDMMC0 command output		
H16	GPIO1_C0/SDMMC0_CLKO	I/O	down	SDMMC0_CLKO	SDMMC0 clock output		
J17	GPIO1_C1/SDMMC0_DET	I/O	up	SDMMC0_DET	SDMMC0 detect input		
J16	GPIO1_C2/SDMMC0_D0/UART2_RX	I/O	up	SDMMC0_D0	SDMMC0 data0 port	UART2_RX	
K17	GPIO1_C3/SDMMC0_D1/UART2_TX	I/O	up	SDMMC0_D1	SDMMC0 data1 port	UART2_TX	
K16	GPIO1_C4/SDMMC0_D2/JTAG_TCK	I/O	up	SDMMC0_D2	SDMMC0 data2 port	JTAG_TCK	
K15	GPIO1_C5/SDMMC0_D3/JTAG_TMS	I/O	up	SDMMC0_D3	SDMMC0 data3 port	JTAG_TMS	
Part I							
G15	GPIO0_B0/SDMMC1_CMD/I2S1_SDO	I/O	up	SDMMC1_CMD	SDIO0 command output, for WIFI module	I2S1_SDO	
F16	GPIO0_B1/SDMMC1_CLKO/I2S1_MCLK	I/O	up	SDMMC1_CLKO	SDIO0 clock output, for WIFI module	I2S1_MCLK	
F17	GPIO0_B3/SDMMC1_D0/I2S1_LRCK_RX	I/O	up	SDMMC1_D0	SDIO0 data port, for WIFI module	I2S1_LRCK_RX	

PIN	Pin Name	Pad type	IO Pull	Default function	Defual function description	Function 2	Function 3
G16	GPIO0_B4/SDMMC1_D1/I2S1_LRCK_TX	I/O	up	SDMMC1_D1	SDIO0 data port, for WIFI module	I2S1_LRCK_TX	
G17	GPIO0_B5/SDMMC1_D2/I2S1_SDI	I/O	up	SDMMC1_D2	SDIO0 data port, for WIFI module	I2S1_SDI	
H15	GPIO0_B6/SDMMC1_D3/I2S1_SCLK	I/O	up	SDMMC1_D3	SDIO0 data port, for WIFI module	I2S1_SCLK	
D17	GPIO1_A0/I2S_MCLK	I/O	down	I2S_MCLK	I2S port		
C17	GPIO1_A1/I2S_SCLK	I/O	down	I2S_SCLK	I2S port		
E15	GPIO1_A2/I2S_LRCK_RX/PWM0	I/O	down	I2S_LRCK_RX	I2S port	PWM0	
D16	GPIO1_A3/I2S_LRCK_TX	I/O	down	I2S_LRCK_TX	I2S port		
D15	GPIO1_A5/I2S_SDI	I/O	down	I2S_SDI	I2S port		
B17	GPIO1_A4/I2S_SDO0	I/O	down	I2S_SDO0	I2S port		
C16	GPIO2_D6/I2S_SDO1	I/O	down	WIFI_REG_ON	WIFI module power enable output		
C15	GPIO2_D5/I2S_SDO2	I/O	down	BT_RST	BT module reset ouput		
B16	GPIO2_D4/I2S_SDO3	I/O	down	SDMMC_PWR	SD card power control output		
Part J							
K5	VCCIO1	P		VCCIO1	CPU IO Power supply		
N10	VCCIO2	P		VCCIO2	CPU IO Power supply		
K13	VCCIO3	P		VCCIO3	CPU IO Power supply		
H13	VCCIO4	P		VCCIO4	CPU IO Power supply		
J5	CVDD1	P		CVDD1	CPU core power supply		
L5	CVDD2	P		CVDD2	CPU core power supply		
N11	CVDD3	P		CVDD3	CPU core power supply		
N12	CVDD4	P		CVDD4	CPU core power supply		
M13	CVDD5	P		CVDD5	CPU core power supply		
L13	CVDD6	P		CVDD6	CPU core power supply		
G13	CVDD7	P		CVDD7	CPU core power supply		
E13	CVDD8	P		CVDD8	CPU core power supply		
E9	CVDD9	P		CVDD9	CPU core power supply		
Part K							
H3	VSS1	G		VSS1	VSS		

PIN	Pin Name	Pad type	IO Pull	Default function	Defual function description	Function 2	Function 3
E10	VSS2	G		VSS2	VSS		
E11	VSS3	G		VSS3	VSS		
E12	VSS4	G		VSS4	VSS		
F6	VSS5	G		VSS5	VSS		
F7	VSS6	G		VSS6	VSS		
F8	VSS7	G		VSS7	VSS		
F9	VSS8	G		VSS8	VSS		
F10	VSS9	G		VSS9	VSS		
F11	VSS10	G		VSS10	VSS		
F12	VSS11	G		VSS11	VSS		
F13	VSS12	G		VSS12	VSS		
G6	VSS13	G		VSS13	VSS		
G7	VSS14	G		VSS14	VSS		
G8	VSS15	G		VSS15	VSS		
G9	VSS16	G		VSS16	VSS		
G10	VSS17	G		VSS17	VSS		
G11	VSS18	G		VSS18	VSS		
G12	VSS19	G		VSS19	VSS		
H6	VSS20	G		VSS20	VSS		
H7	VSS21	G		VSS21	VSS		
H8	VSS22	G		VSS22	VSS		
H9	VSS23	G		VSS23	VSS		
H10	VSS24	G		VSS24	VSS		
H11	VSS25	G		VSS25	VSS		
H12	VSS26	G		VSS26	VSS		
J6	VSS27	G		VSS27	VSS		
J7	VSS28	G		VSS28	VSS		
J8	VSS29	G		VSS29	VSS		

PIN	Pin Name	Pad type	IO Pull	Default function	Defual function description	Function 2	Function 3
J9	VSS30	G		VSS30	VSS		
J10	VSS31	G		VSS31	VSS		
J11	VSS32	G		VSS32	VSS		
J12	VSS33	G		VSS33	VSS		
J13	VSS34	G		VSS34	VSS		
K6	VSS35	G		VSS35	VSS		
K7	VSS36	G		VSS36	VSS		
K8	VSS37	G		VSS37	VSS		
K9	VSS38	G		VSS38	VSS		
K10	VSS39	G		VSS39	VSS		
K11	VSS40	G		VSS40	VSS		
K12	VSS41	G		VSS41	VSS		
L6	VSS42	G		VSS42	VSS		
L7	VSS43	G		VSS43	VSS		
L8	VSS44	G		VSS44	VSS		
L9	VSS45	G		VSS45	VSS		
L10	VSS46	G		VSS46	VSS		
L11	VSS47	G		VSS47	VSS		
L12	VSS48	G		VSS48	VSS		
M6	VSS49	G		VSS49	VSS		
M7	VSS50	G		VSS50	VSS		
M8	VSS51	G		VSS51	VSS		
M9	VSS52	G		VSS52	VSS		
M10	VSS53	G		VSS53	VSS		
M11	VSS54	G		VSS54	VSS		
M12	VSS55	G		VSS55	VSS		
J1	VSS56	G		VSS56	VSS		

Notes:

Ⓜ: Pad types: I = input, O = output, I/O = input/output (bidirectional)

*AP = Analog Power, AG = Analog Ground
DP = Digital Power, DG = Digital Ground
A = Analog*

- ②: Output Drive Unit is mA, only Digital IO has drive value;*
- ③: Reset state: I = input without any pull resistor, O = output without any pull resistor;*
- ④: In RK3036G, all the IOs are in the same power supply;*
- ⑤: NC: not connect;*
- ⑥: Driver strength for these IOs is configurable; others are fixed and determined by IO type.*

Rockchip Confidential

2.7 IO pin name descriptions

This sub-chapter will focus on the detailed function description of every pins based on different interface.

Table 2-4 RK3036G IO function description list

Interface	Pin Name	Direction	Description
Misc	XIN24M	I	Clock input of 24MHz crystal
	XOUT24M	O	Clock output of 24MHz crystal
	NPOR	I	Chip hardware reset
SWJ-DP	jtag_tck	I	JTAG interface clock input/SWD interface clock input
	jtag_tms	I/O	JTAG interface TMS input/SWD interface data out
SD/MMC Host Controller	sdmmc0_clkout	O	sdmmc card clock
	sdmmc0_cmd	I/O	sdmmc card command output and response input
	sdmmc0_data <i>i</i> (<i>i</i> =0~3)	I/O	sdmmc card data input and output
	sdmmc0_detect_n	I	sdmmc card detect signal, 0 represents presence of card
SDIO Host Controller	sdio_clkout	O	sdio card clock
	sdio_cmd	I/O	sdio card command output and response input
	sdio_data <i>i</i> (<i>i</i> =0~3)	I/O	sdio card data input and output
eMMC Interface	emmc_clkout	O	emmc card clock
	emmc_cmd	I/O	emmc card command output and response input
	emmc_data <i>i</i> (<i>i</i> =0~7)	I/O	emmc card data input and output
DMC	DDR_CK	O	Active-high clock signal to the memory device
	DDR_CK_N	O	Active-low clock signal to the memory device
	DDR_CKE <i>i</i>	O	Active-high clock enable signal to the memory device for two chip select
	DDR_CSN <i>i</i> (<i>i</i> =0,1)	O	Active-low chip select signal to the memory device. There are two chip select
	DDR_RASN	O	Active-low row address strobe to the memory device
	DDR_CASN	O	Active-low column address strobe to the memory device
	DDR_WEN	O	Active-low write enable strobe to the memory device
	DDR_BA[2:0]	O	Bank address signal to the memory device
	DDR_ADDR[15:0]	O	Address signal to the memory device
	DDR_DQ[15:0]	I/O	Bidirectional data line to the memory device.
	DDR_DQS[3:0]	I/O	Active-high bidirectional data strobes to the memory device
	DDR_DQS_B[3:0]	I/O	Active-low bidirectional data strobes to the memory device
	DDR_DM[3:0]	O	Active-low data mask signal to the memory device
	DDR_ODT <i>i</i> (<i>i</i> =0,1)	O	On-Die Termination output signal for two chip select
	DDR_RESET	O	DDR3 reset signal to the memory device
NandC	flash_wp	O	Flash write-protected signal
	flash_ale	O	Flash address latch enable signal
	flash_cle	O	Flash command latch enable signal
	flash_wrn	O	Flash write enable and clock signal

Interface	Pin Name	Direction	Description
	flash_rdn	O	Flash read enable and write/read signal
	flash_data <i>i</i> (<i>i</i> =0~7)	I/O	Flash data inputs/outputs signal
	flash_rdy	I	Flash ready/busy signal
	flash_csn0	O	Flash chip enable signal for chip0
SFC	sfc_clk	O	Serial flash clock
	sfc_csni(<i>i</i> =0,1)	O	Serial flash chip enable signal for chip <i>i</i> (<i>i</i> =0,1)
	sfc_sioi(<i>i</i> =0~3)	I/O	Serial flash data inputs/outputs signal
I2S/PCM Controller	i2s_clk	O	I2S/PCM clock source
	i2s_sclk	I/O	I2S/PCM serial clock
	i2s_lrckrx	I/O	I2S/PCM left & right channel signal for receiving serial data, synchronous left & right channel in I2S mode and the beginning of a group of left & right channels in PCM mode
	i2s_lrcktx	I/O	I2S/PCM left & right channel signal for transmitting serial data, synchronous left & right channel in I2S mode and the beginning of a group of left & right channels in PCM mode
	i2s_sdi	I	I2S/PCM serial data input
	i2s_sdoi(<i>i</i> =0~3)	O	I2S/PCM serial data output
SPDIF transmitter	spdif_tx	O	SPDIF biphas data ouput
SPI Controller	spi_clk	I/O	SPI serial clock
	spi_csni(<i>i</i> =0,1)	I/O	SPI chip select signal,low active
	spi_txd	O	SPI serial data output
	spi_rxd	I	SPI serial data input
PWM	pwm3	O	Pulse Width Modulation output
	pwm2	O	Pulse Width Modulation output
	pwm1	O	Pulse Width Modulation output
	pwm0	O	Pulse Width Modulation output
I2C	i2c0_sda	I/O	I2C0 data
	i2c0_scl	I/O	I2C0 clock
	i2c1_sda	I/O	I2C1 data
	i2c1_scl	I/O	I2C1 clock
	i2c2_sda	I/O	I2C2 data
	i2c2_scl	I/O	I2C2 clock
UART	uart0_sin	I	UART0serial data input
	uart0_sout	O	UART0serial data output
	uart0_ctsn	I	UART0 clear to send
	uart0_rtsn	O	UART0 request to send
	uart1_sin	I	UART1serial data input
	uart1_sout	O	UART1serial data output
	uart2_sin	I	UART2serial data input
	uart2_sout	O	UART2serial data output
EMAC	mac_clk	I/O	RMII REC_CLK output or EMAC external clock input
	mac_mdc	O	EMAC management interface clock
	mac_mdio	I/O	EMAC management interface data
	mac_txdi(<i>i</i> =0~1)	O	EMAC TX data

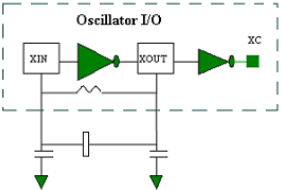
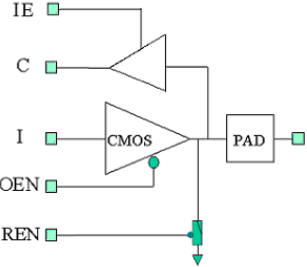
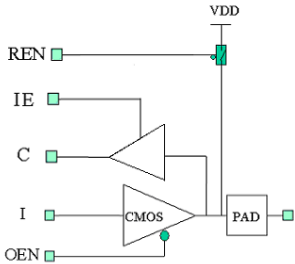
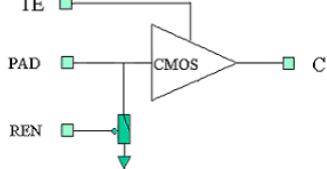
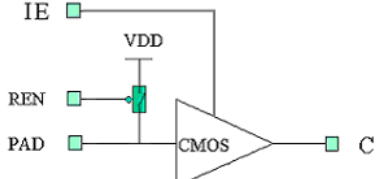
Interface	Pin Name	Direction	Description
	max_rxd <i>i</i> (<i>i</i> =0~1)	I	EMAC RX data
	mac_txen	O	EMAC TX data enable
	mac_rxer	I	EMAC RX error signal
	mac_crs	I	PHY CRS signal
USB OTG 2.0	USB0PP	I/O	USB OTG 2.0 Data signal DP
	USB0PN	I/O	USB OTG 2.0 Data signal DM
	USB0ID	I	USB OTG 2.0 ID indicator
	VBUS_0	N/A	USB OTG 2.0 5V power supply pin
USB Host 2.0	USB1PP	I/O	USB HOST 2.0 Data signal DP
	USB1PN	I/O	USB HOST 2.0 Data signal DM
	VBUS_1	N/A	USB HOST 2.0 5V power supply pin
	USBRBIAS	N/A	45 Ohm Reference external resistance
eFuse	EFUSE_AVDD	N/A	eFuse program and sense power
HDMI	EXTR	O	Connect 2.0Kohm resistor to ground to generate reference current
	TX0N	O	TMDS channel 0 negative data line
	TX0P	O	TMDS channel 0 positive data line
	TX1N	O	TMDS channel 1 negative data line
	TX1P	O	TMDS channel 1 positive data line
	TX2N	O	TMDS channel 2 negative data line
	TX2P	O	TMDS channel 2 positive data line
	TX3N	O	TMDS negative clock line
Audio CODEC	VCM	I	Reference voltage input
	VOUTL	O	Left channel headphone output
	VOUTR	O	Right channel headphone output
Video DAC	IREF	I/O	Reference current. Output current when using External Reference Resistor or Input Reference Current when using external current source
	IOUTP0	O	Positive output
	IOUTN0	O	Negative output

2.8 IO Type

The following list shows IO type except DDR IO and all of Power/Ground IO.

Table 2-5 RK3036G IO Type List

Type	Diagram	Description	Pin Name
A		Analog IO Cell with IO voltage	EFUSE_VQPS
B		Dedicated Power supply to Internal Macro with IO voltage	SARADC_AIN[2:0]

Type	Diagram	Description	Pin Name
C		Crystal Oscillator with high enable	XIN24M/XOUT24M
D		CMOS 3-state output pad with controllable input and controllable pulldown	Part of digital GPIO (PBCDxRN)
E		CMOS 3-state output pad with controllable input and controllable pullup	Part of digital GPIO (PBCUxRN)
F		controllable input pad with controllable pulldown	Part of digital GPIO (PICDRN)
G		controllable input pad with controllable pullup	Part of digital GPIO (PICURN)

Chapter 3 Electrical Specification

3.1 Absolute Maximum Ratings

Table 3-1 RK3036G absolute maximum ratings

Parameters	Related Power Group	Max	Unit
DC supply voltage for Internal digital logic	CVDD, HDMI_DVDD1V1_1, HDMI_DVDD1V1_2, HDMI_DVDD1V1_3, HDMI_DVDD1V1_4 USB_DVDD11	1.4	V
DC supply voltage for Digital GPIO (except for PLL, USB, DDR, ACODEC, VDAC. HDMI IO)	VCCIO	3.63	V
DC supply voltage for DDR IO	DDR_VDD	1.575	V
DC supply voltage for Analog part of PLL	PLL_VCCIO	3.63	V
DC supply voltage for Analog part of PLL	APLL_DVDD11,DPLL_DVDD11	1.21	V
DC supply voltage for Analog part of USB OTG/Host2.0	USB_AVDD33	3.63	V
DC supply voltage for Analog part of HDMI	HDMI_AVDD33	3.63	V
Analog Input voltage for DP/DM/VBUS of USB OTG/Host2.0		5.25	V
Digital input voltage for input buffer of GPIO		3.63	V
Digital output voltage for output buffer of GPIO		3.63	V
Storage Temperature	Tstg	125	°C
Max Conjunction Temperature	Tj	125	°C

Absolute maximum ratings specify the values beyond which the device may be damaged permanently. Long-term exposure to absolute maximum ratings conditions may affect device reliability.

3.2 Recommended Operating Conditions

Following table describes the recommended operating condition.

Table 3-2 RK3036G recommended operating conditions

Parameters	Symbol	Min	Typ	Max	Units
Max frequency of CPU	Frequency			1.0	GHz
Max frequency of GPU	Frequency			400	MHz
Internal digital logic Power	CVDD, HDMI_DVDD1V1_1, HDMI_DVDD1V1_2, HDMI_DVDD1V1_3, HDMI_DVDD1V1_4 USB_DVDD11	0.99	1.1	TBD	V
Digital GPIO Power(3.3V)	VCCIO	2.97	3.3	3.63	V
DDR IO (DDRIII mode) Power	DDR_VDD	1.425	1.5	1.575	V
DDR IO (LVDDRIII mode) Power	DDR_VDD	1.28	1.35	1.45	V
PLL Analog Power	PLL_VCCIO	2.97	3.3	3.63	V
PLL Analog Power	APLL_DVDD11,DPLL_DVDD11	0.99	1.1	1.21	V
USB OTG/Host2.0 Analog Power(3.3V)	USB_AVDD33	2.97	3.3	3.63	V
USB OTG/Host2.0 external resistor	REXT	40.5	45	49.5	Ohm
Acodec Analog Power	CODEC_AVDD	2.97	3.3	3.63	V
HDMI Analog Power	HDMI_AVDD33	2.97	3.3	3.63	V
EFUSE programming voltage		N/A	2.5	N/A	V
PLL input clock frequency		N/A	24	N/A	MHz
Ambient Operating Temperature ②	Ta	0	25	80	°C

Notes : ① Symbol name is same as the pin name in the io descriptions

② with the reference software setup, the reference software will limit the chipset temperature about 80 °C

Table 3-3 RK3036G DC Characteristics

Parameters		Symbol	Min	Typ	Max	Units
Digital GPIO @3.3V	Input Low Voltage	V _{IL}	-0.3		0.8	V
	Input High Voltage	V _{IH}	2		VDD25+0.3	V
	Output Low Voltage	V _{OL}			0.4	V
	Output High Voltage	V _{OH}	2.4			V
	Threshold point	V _T	1.31	1.55	1.83	V
	Schmitt trig Low to High threshold point	V _{T+}	1.42	1.75	1.98	V
	Schmitt trig. High to Low threshold point	V _{T-}	1.11	1.30	1.52	V
	Pullup Resistor	R _{PU}	27	41	64	Kohm
	Pulldown Resistor	R _{PD}	31	46	78	Kohm
DDR IO @DDR3 mode	Input High Voltage	V _{ih_dds}	VREFi + 0.125 (i=0~2)	1.5	VDDIO_DDRi + 0.3 (i=0~6)	V
	Input Low Voltage	V _{il_dds}	-0.3	0	VREFi - 0.125 (i=0~2)	V
	Output High Voltage	V _{oh_dds}	VDDIO_DDRi - 0.28 (i=0~6)	1.5	N/A	V
	Output Low Voltage	V _{ol_dds}	N/A	0	0.28	V
	Input termination resistance(ODT) to VDDIO_DDRi/2 (i=0~6)	R _{tt}	120 60 40	150 75 50	180 90 60	Ohm
HDMI	Single-ended high level output voltage, (when sink <=165Mhz)	V _H	HDMI_AVDD 33-10mv		HDMI_AVDD 33+10mv	mv
	Single-ended high level output voltage, (when sink >165Mhz)	V _H	HDMI_AVDD 33-200mv		HDMI_AVDD 33+10mv	mv
	Single-ended low level output voltage, (when sink <=165Mhz)	V _L	HDMI_AVDD 33-600mv		HDMI_AVDD 33-400mv	mv
	Single-ended low level output voltage, (when sink >165Mhz)	V _L	HDMI_AVDD 33-700mv		HDMI_AVDD 33-400mv	mv
	Single-ended output swing voltage	V _{s wing}	400		600	mv
	Single-ended standby (off) output voltage	V _{OFF}		HDMI_AVDD 33+10mv		mv
	Single-ended standby (off) output current	I _{OFF}	-10		10	uA
PLL	Input High Voltage	V _{ih_pll}	0.8*DVDD_i PLL (i=A,D,G)	DVDD_iPLL (i=A,D,G)	DVDD_iPLL (i=A,D,G)	V
	Input Low Voltage	V _{il_pll}	0	0	0.2*DVDD_i PLL (i=A,D,G)	V
VDAC	High voltage analog supply		3.0	3.3	3.6	V
	Digital supply voltage		0.99	1.1	1.21	V

3.3 Recommended Operating Frequency

Table 3-4 Recommended operating frequency for PD_BUS domain

Parameter	Condition	Symbol	MIN	TYP	MAX	Unit
DDR PLL	1.0V , 25 °C	ddr_pll_clk			1600	MHz
	1.1V , -40 °C					
	0.9V , 125 °C		800			
ARM PLL	1.0V , 25 °C	arm_pll_clk			1600	MHz
	1.1V , -40 °C					
	0.9V , 125 °C		900			
GENERAL PLL	1.0V , 25 °C	general_pll_clk			1400	MHz

Parameter	Condition	Symbol	MIN	TYP	MAX	Unit
	1.1V , -40 °C					
	0.9V , 125 °C		600			

3.4 Electrical Characteristics for General IO

Table 3-5 RK3036G Electrical Characteristics for Digital General IO

Parameters		Symbol	Test condition	Min	Typ	Max	Units
Digital GPIO @3.3V	Input leakage current	I _L	V _{in} = 3.3V or 0V			±10	uA
	Tri-state output leakage current	I _{oz}	V _{out} = 3.3V or 0V			±10	uA
	High level input current	L _{IH}	V _{in} = 3.3V, pulldown disabled				mA
			V _{in} = 3.3V, pulldown enabled				mA
	Low level input current	L _{IL}	V _{in} = 0V, pullup disabled				mA
			V _{in} = 0V, pullup enabled				mA

3.5 Electrical Characteristics for PLL

Table 3-6 RK3036G Electrical Characteristics for PLL

Parameters		Symbol	Test condition	Min	Typ	Max	Units
PLL	Input clock frequency(Int)	F _{in}	F _{in} = FREF @3.3V/1.1V	1		800	MHz
	Input clock frequency(Frac)	F _{in}	F _{in} = FREF @3.3V/1.1V	10		800	MHz
	Comparison frequency	F _{ref}	FREF = F _{in} /REFDIV @3.3V/1.1V	1		40	MHz
	VCO operating range	F _{vco}	Fvco = Fref * FBDIV @3.3V/1.1V	400		1600	MHz
	Output clock frequency	F _{out}	Fout = Fvco/POSTDIV @3.3V/1.1V	1		1600	MHz
	Lock time	T _{lt}	@ 3.3V/1.1V, FREF=24M,REFDIV=1		1000	1500	Inputclockcycles
	VDDHV current consumption		Fvco = 1000MHz, @3.3V, 25 °C Current scale as (Fvco/1GHz) ^{1.5}		0.8	1.0	mA
	VDD Power consumption (normal mode)		@3.3V/1.1V, 25 °C		3	4	uW/MHz
	Power consumption (bypass mode)		BYPASS=HIGH , PD=LOW , F _{in} = 24MHz, F _{out} = 24MHz, @3.3V/1.1V, 25 °C				uW
	Power consumption (power-down mode)		PD=HIGH, @27 °C		10		uA

Notes :

①:REFDIV is the input divider value;

FBDIV is the feedback divider value;

POSTDIV is the output divider value

3.6 Electrical Characteristics for USB Interface

Table 3-7 RK3036G Electrical Characteristics for USB Interface

Parameters		Symbol	Test condition	Min 2xport	Typ 2xport	Max 2xport	Units
USB	Supply current, low speed		IDLE USB_AVDD33 = 3.3V USB_DVDD12 = 1.1V	24	26	29	mA

Parameters	Symbol	Test condition	Min 2xport	Typ 2xport	Max 2xport	Units
		TX USB_AVDD33 = 3.3V USB_DVDD12 = 1.1V	45	48	50	mA
		RX USB_AVDD33 = 3.3V USB_DVDD12 = 1.1V	40	43	46	mA
Supply current, full speed		IDLE USB_AVDD33 = 3.3V USB_DVDD12 = 1.1V	25	28	30	mA
		TX USB_AVDD33 = 3.3V USB_DVDD12 = 1.1V	55	59	63	mA
		RX USB_AVDD33 = 3.3V USB_DVDD12 = 1.1V	50	52	54	mA
Supply current, high speed		IDLE USB_AVDD33 = 3.3V USB_DVDD12 = 1.1V	33	35	38	mA
		TX USB_AVDD33 = 3.3V USB_DVDD12 = 1.1V	65	69	73	mA
		RX USB_AVDD33 = 3.3V USB_DVDD12 = 1.1V	50	54	56	mA
Supply current, suspend		USB_AVDD33 = 3.3V USB_DVDD12 = 1.1V		20	32	uA

3.7 Electrical Characteristics for DDR IO

Table 3-8 RK3036G Electrical Characteristics for DDR IO

Parameters	Symbol	Test condition	Min	Typ	Max	Units
DDR IO @DDR3 mode	VDDIO_DDR standby current, ODT OFF	@ 1.5V , 125°C				uA
	Input leakage current, SSTL mode, unterminated	@ 1.5V , 125°C				uA
DDR IO @LVDDR3 mode	Input leakage current	@ 1.35V,125°C				uA
	VDDquiescent current	@ 1.35V,125°C				uA

3.8 Electrical Characteristics for eFuse

Table 3-9 RK3036G Electrical Characteristics for eFuse

Parameters	Symbol	Test condition	Min	Typ	Max	Units
Standby current	I _{standby}		-	1	-	uA
Peak burning current	I _{prog}		-	15	-	mA
Current during normal reading	I _{active}	10MHz	-	4	-	mA

3.9 Electrical Characteristics for HDMI

Table 3-10 RK3036G Electrical Characteristics for HDMI

Parameters	Symbol	Test condition	Min	Typ	Max	Units
Rise time/fall time (20%-80%)			75		0.4*T _{bit}	ps
Overshoot, max			15% of full differential amplitude (V _{swing} *2)			mv
Undershoot, max			20% of full differential amplitude (V _{swing} *2)			mv
Intra-Pair Skew at Transmitter Connector, max			0.15 * T _{bit}			ps
Inter-Pair Skew at Transmitter Connector, max			0.20 * T _{bit}			ps
TMDS Differential Clock Jitter, max			0.25 * T _{bit}			ps
Clock duty cycle			40%		60%	

3.10 Electrical Characteristics for VDAC

Table 3-11 RK3036G Electrical Characteristics for VDAC

Parameters	Symbol	Test condition	Min	Typ	Max	Units
High voltage analog current consumption		I _{fs} =34mA		51		mA
Digital current consumption		F _s =300MHz		0.7		mA
Current consumption in power down, analog					10	μA
Current consumption in power down, digital					50	μA

Chapter 4 Thermal Management

4.1 Overview

For reliability and operability concerns, the absolute maximum junction temperature of RK3036G has to be below 125□.

4.2 Package Thermal Characteristics

Table 4-1 provides the thermal resistance characteristics for the package used on RK3036G. The resulting simulation data for reference only, please prevail in kindtest.

Table 4-1 RK3036G Thermal Resistance Characteristics

Package (TFBGA236)	Power(W)	θ_{JA} (°C/W)	θ_{JB} (°C/W)	θ_{JC} (°C/W)
RK3036G	1	37	25.7	6.8

Note: The testing PCB is base on 4 layers, 114.3mmx 101.6mm, 1.6 mm Thickness, Ambient temperature is 40 ° C.