Product Selection Guide

Pangomirco Ltd.

V4.0-2022.2

Overview

Pangomirco Ltd. is the leading FPGA vendor in China with investment amount of more than 4 billion RMB and registered capital of 500 million RMB.

We are specialized in development of Programmable Logic Devices (including FPGA and CPLD) for more than 10 years and we have been devoted to providing programmable platform & system solution in various application areas, including Communication, Industrial, Video Processing, Consumer, Data Center, High-Performance Computing etc. With overall more than 600 employees, 90% of which are R&D,we have nearly 300 patents, 80% of them are patent for invention and software.

Shenzhen HQ
R&D, Operation and Marketing Center

Shanghai Branch
R&D, Sales

Beijing Branch
R&D, Sales

Chengdu Branch
R&D,Sale

Milestones

2013

Dec, Pangoelectronics Ltd. officially founded

2014

Feb，Shanghai branch founded
Sep, Chengdu branch founded

2015

Nov，Titan FPGA PGT30G launched, first 30K-LE level device in China

2016

Sep，Titan FPGA PGT180H launched, first 180K-LE level device in China

2017

Oct, Logos FPGA family launched

2018

Oct，Compa CPLD family launched

2019

Revenue over 100 million RMB

2020

28nm Logos-2 100K-LE device went to production;
Revenue over 300 million RMB

2021

28nm Titan-2 400K-LE device went to production;
Revenue over 700 million RMB

Compa

Low Power CPLD

Compa CPLD Device Family uses 55nm eFlash process and independent LUT5 architecture, suitable for low-power, low-cost, small form factor applications, ideal for IO expansion, IO bridging, board management functions. It is widely used in Communication, Industrial and Consumer markets.

Features

- 55nm eFlash process, non-volatile device
- 1K~10K LUT4 logic elements，3.3/2.5V core voltage or 1.2V core voltage supported
- MIPI、LVDS、I2C、SPI、OSC、RAM、PLL
- RAM Soft-Error detection and correction
- Dual Boot function with no external Flash
- Back-stage upgrade supported, read-back banned
- Max User IO up to 384
- Package size down to 2.5x2.5mm

	Part Number[1]	PGC1K	PGC2K	PGC4K	PGC7K	PGC10K
LE	Equivalent LUT4	1276	2428	4761	7104	9907
	Flip-Flop	1596	3036	5952	8880	12384
RAM	Distributed RAM(Kbit)	11	16	39	56	78
	DRM(9Kbit/pcs)	7	8	11	26	45
	DRM(Kbit)	63	72	99	234	405
Flash	UFM[2]	350	80	1520	2070	3016
Clock	PLL/Global Clock	1/16	2/16	2/16	2/16	2/16
IO	IO Banks	4	6	6	6	6
	Max User I/O	207	207	280	336	384
	Max Diff I/O(Pair)	14	14	18	21	24
Hardcore	I2C	2	2	2	2	2
	SPI	1	1	1	1	1
	Counter	1	1	1	1	1
	OSC	1	1	1	1	1

Package	Size(mm)	Pitch(mm)	User IO/Diff IO				
UWG36[4]	2.5 x 2.5	0.4	29/3 [3]				
UWG49	3.2 x 3.2	0.4		39/5			
UWG81	3.8 x 3.8	0.4			64/10		
SSBG256	9 x 9	0.5		207/14	207/14		
LPG100	14 x 14	0.5	80/4	80/4			
LPG144	20 x 20	0.5	112/4	112/4	115/9	115/9	
MBG256	14 x 14	0.8	207/14	207/14	207/18	207/19	
FBG256	17 x 17	1.0	207/14	207/14	207/18		
MBG324	15 x 15	0.8			280/18		
MBG400	17 x 17	0.8				336/21	
FBG484	23 x 23	1.0				335/21	
MBG484	19 x 19	0.8					384/24

Note:1.PGC1K/PGC2K include G-type(General) and L-type(Low-power); PGC4K includes L-type and D-type(Dual-Boot); PGC7K/PGC10K include D-type
2.UFM(User Flash Memory) means the user available Flash memory without extra bitstream for Dual-Boot function
3.29/3 represents 29 user I/O, 3 pairs of Differential IO, the same with other number pairs
4.UWG and SSBG packages are only available for 1.2V low-power devices

Logos

Cost Effective FPGA

Logos FPGA family uses 40nm CMOS process and new LUT5 architecture. It supports rich IO and on-chip resources like RAM, DSP, ADC, Serdes and DDR3. It is widely used in Communication, Industrial, Consumer markets, and ideal for high volume, cost sensitive applications.

Features

- 40nm process, low power, low cost
- 12K~100K LUTs
- Flexible CLM
- RAM Soft-Error detection and correction
- DDR3 800Mbps
- Multiple IO standard，LVDS、MIPI supported
- LVDS up to 800Mbps
- SERDES up to 6.375Gbps
- ADC hardcore integrated
- Advanced 256-bit AES encryption

	Part Number	PGL12G	PGL22G	PGL22GS	PGL25G	PGL50G	PGL50H	PGL100H
LE	Equivalent LUT4	12480	21043	21043	27072	51360	51360	102451
	Flip-Flops	15600	26304	26304	33840	64200	64200	128064
RAM	RAM(Kbit)	84	71	71	242	544	544	993
	DRM(18Kbit/pcs)	30	48	48	60	134	134	286
	DRM(Kbit)	540	864	864	1080	2412	2412	5148
Clock	PLL	4	6	6	4	5	5	8
IO	Max User IO	160	240	140	308	341	304	498
	Max Diff IO(pair)	80	120	68	154	170	152	249
	DDR3 (Mbps)	800	800#	800	800	800	800	800
Hardcore	APM(18*18)	20	30	30	40	84	84	188
	ADC	1	1	—	—	—	—	—
	PCIe Gen2x4	—	—	—	—	—	1	1
	AES	1	1	1	—	1	1	1
	HSST(6.375Gbps)	—	—	—	—	—	4	8

Package	Size(mm)	Pitch(mm)	User IO/Diff IO/HSST						
LPG144	22 x 22	0.5	103/51/0						
FBG256	17 x 17	1.0	160/80/0	186/93/0		186/93/0			
MBG324	15 x 15	0.8		240/120/0		226/113/0			
LPG176	22 x 22	0.4			140/68/0				
FBG484	23 x 23	1.0				308/154/0	332/170/0	296/148/4	
FBG900	31 x 31	1.0							498/249/8

Note：1、#"represents that the device supports DDR3

Logos-2

New Generation of Cost Effective FPGA

Logos-2 uses high performance 28nm CMOS process，with LE ranging from 25K~200K. It supports rich on-chip resources and high-performance interface like SerDes, DDR3, and PCIe. Comparing to the previous generation, Logos-2 achieves 50% higher performance with 40 % lower power. Logos-2 is ideal for high volume, low-power, high-performance applications. It is widely used in Communication, Video Processing, Industrial, Test & Measurement, and Medical markets.

Features

- High performance 28nm process
- 25K~200K LUTs
- Flexible CLM
- SerDes up to 6.6Gbps
- HardcorePCIe Gen2x4
- DDR3up to 1066Mbps
- RAM Soft-Error detection and correction
- Flexible IO interfaces, LVDS、MIPI、TMDS supported, LVDS up to 1.25Gbps
- ADC hardcore integrated with12bit resolution and 1MSPS
- Advanced 256-bit AES encryption

	Part Number	PG2L25H	PG2L50H	PG2L100H	PG2L200H
LE	Equivalent LUT4	26700	53700	99900	232800
	Flip-Flops	35600	71600	133200	356800
RAM	Distributed RAM(Kbit)	352	742	1273	2944
	DRM(36Kbit/pcs)	55	85	155	415
	DRM(Kbit)	1980	3060	5580	14940
Clock	GPLL+PPLL	3+3	5+5	6+6	10+10
IO	Max User IO	150	250	300	500
	Max Diff IO(pair)	72	120	144	240
	DDR3(Mbps)	1066	1066	1066	1066
Hardcore	APM(25*18)	80	120	240	740
	ADC	1	1	1	1
	PCIe Gen2x4	1	1	1	1
	AES	1	1	1	1
	HSST(6.6Gbps)	4	4	8	16

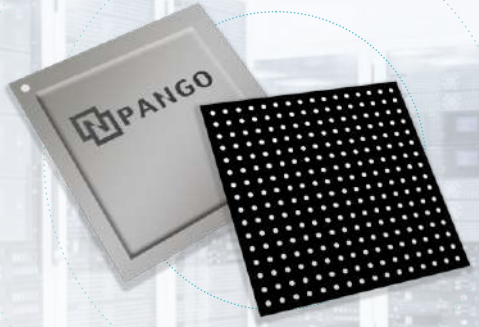
Package	Size(mm)	Pitch(mm)	User IO/HSST			
SBG236	10 x 10	0.5		106/2		
SBG238	10 x 10	0.5	112/2			
FBG256	17 x 17	1.0		170/0		
MBG324	15 x 15	0.8		210/0	210/0	
MBG325	15 x 15	0.8	150/4	150/4		
FBG484[1]	23 x 23	1.0		250/4	285/4	
FBB484[1]	23 x 23	1.0				285/4
MBB484	19 x 19	0.8				285/4
FBG676[2]	27 x 27	1.0			300/8	
FBB676[2]	27 x 27	1.0				400/8
FFBG1156	35 x 35	1.0				500/16

Note:1.FBG484 and FBB484 pin-to-pin compatible 2.FBG676 and FBB676 pin-to-pin compatible

Titan-2

New Generation of High End FPGA

Titan-2 FPGA family uses high performance 28nm CMOS process. Titan-2 has logic density up to 390K and supports SerDes high-speed interface, PCIe Gen3 , DDR3/4, providing high-performance programmable solutions. It is widely used in Communication, Video Processing, Industrial, Test & Measurement markets.



Features

- Up to 390K Logic Cell
- Serdes up to 13.125Gbps
- High bandwidth，DDR4 1866Mbp
- RAM Soft-Error detection and correction
- Hardcore PCIe Gen3x8
- Multiple high-speed IO interfaces: LVDS, MIPI, LVDS up to 1.4Gbps
- ADC hardcore integrated with 12bit resolution and 1MSPS
- Advanced 256-bit AES encryption

	Part Number	PG2T90H	PG2T210H	PG2T390H
LE	Logic Cell	90K	210K	390K
	Flip-Flops	109K	260K	487K
RAM	Distributed RAM(Kbit)	1240	2688	4712
	DRM(36Kbit/pcs)	150	340	480
	DRM(Kbit)	5400	12240	17280
Clock	GPLL+PPLL	6+6	8+8	10+10
IO	Max User IO	300	400	500
	Max Diff(pair)	144	192	240
	DDR3/4 (Mbps)	1866	1866	1866
Hardcore	APM(25*18)	240	600	840
	ADC	1	1	1
	PCIe Gen3x8	1	1	1
	AES	1	1	1
	HSST (13.125Gbps)	8	8	16

Package	Size(mm)	Pitch(mm)	HR_IO/HP_IO/HSST[1]		
FBB484	23 x 23	1.0	185/100/4	185/100/4	
FBB676[2]	27 x 27	1.0	200/100/8	250/150/8	
FFBG676[2]	27x 27	1.0		250/150/8	250/150/8
FFBG900	31 x 31	1.0			350/150/16

Note:1.HR_IO represents high-range IO, HP_IO represents High-Performance IO 2. FBB676 and FFBG676 pin-to-pin compatible

PN Description

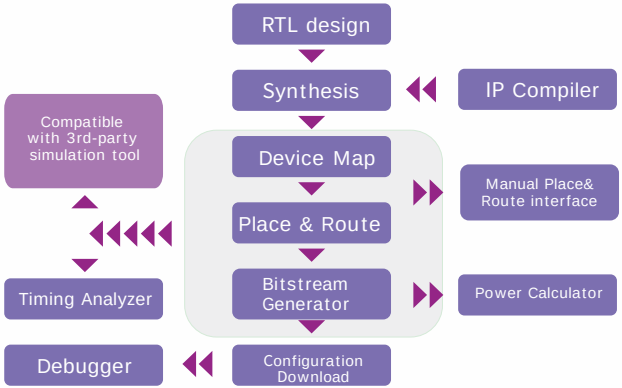
Titan-2	**PG**	**2T**	**90**	**H**	–	**6**	**C**	**FBB**	**484**
	PANGO	Titan-2	LE 90-390K	H: with serdes G: without serdes		5: low speed 6: mid speed 7: high speed	Operation Temperature C=Commercial(Tj=0°Cto+85°C) I=Industrial(Tj= -40°Cto+100°C)	Package FBB/FFBG	Pin Count 484/676/900
Logos	**PG**	**L**	**22**	**G**	–	**6**	**I**	**FBG**	**256**
	PANGO	Logos	LE 12K-100K	H: with serdes G: without serdes GS: with SDRAM		5: low speed 6: mid speed 7: high speed	Operation Temperature C=Commercial(Tj=0°Cto+85°C) I=Industrial(Tj= -40°Cto+100°C)	Package LPG/MBG/FBG	Pin Count 144/176/256 /324/484/900
Logos-2	**PG**	**2L**	**100**	**H**	–	**6**	**I**	**FBG**	**676**
	PANGO	Logos-2	LE 25K-200K	H: with serdes G: without serdes		5: low speed 6: mid speed 7: high speed	Operation Temperature C=Commercial(Tj=0°Cto+85°C) I=Industrial(Tj= -40°Cto+100°C)	Package SBG/MBG/FBB/ MBB/FFBG/FBG	Pin Count 236/238/256/324/ 325/484/676/1156
Compa	**PG**	**C**	**2K**	**G**	–	**6**	**I**	**FBG**	**256**
	PANGO	Compa	LE 1K-10K	G: General L: low power D: Dual Boot		5: low speed 6: mid speed 7: high speed	Operation Temperature C=Commercial(Tj=0°Cto+85°C) I=Industrial(Tj= -40°Cto+100°C)	Package UWG/SSBG/ FBG/LPG/MBG	Pin Count 36/49/81/100/144/ 256/324/332/400/484

PDS

Pango Design Suite (PDS) is a software design tool developed by Pango with independent property rights. In order to provide highly efficient and user-friendly design environment for entire device portfolio, PDS covers the whole design flow from RTL description to configuration download. PDS is compatible to standard design flow and currently capable to handle design on 1000K-LE level.

Feature

1. Fast-running software, simple UI, reliable performance
2. Customizable IP integrated
3. Innovative place & route algorithm for various kinds of design
4. High-efficient independent synthesis tool for optimized HDL solution
5. Multi-dimensional report and graphics to demenstrated key parameters
6. Expandable debug tool and model for quick diagnostic on user design



IP & Solution

Storage
PSRAM
DDR4
DDR3
SATA
DRM
eMMC
SDIO
•••

COMM
XAUI
SGMII
QSGMII
Interlaken
TS MAC
10G EMAC
•••

Interface
PCIe 3.0
PCIe 2.0
LVDS
CAN
SERDES/HSST
UART
iScan
•••

Video
Display Port
SDI
MIPI
Harden D-PHY
DSC
HDMI
V-By-One
•••

Others
Cortex M1
JESD204B
Divider
SEU
ADC
APM
PLL
•••

Boards

Compa	Logos	Logos-2	Titan-2

PGC2K
Eva Board

PGL22G
Eva Board

PGL12G
Eva Board

PGL25G
Eva Board

PG2L100H
Eva Board

ALINX PG2T390H AXP390
Core & Eva Board

ALINX PGC7KD
Eva Board

PGL50H
Eva Board

PGL50H
Eva Board

ALINX PGL12G
Eva Board

ALINX PG2L100H AXP100
Core & Eva Board

ALINX PGL22
Eva Board

ALINX PGL22G P1
Logic Analyzer

ALINX PGL50H AXP50
Experiment Box

灵活编程 同创未来

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