



SIM8950 Series I2C Driver Development Guide Manual_V1.00.01

Smart Module

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Version History

Version	Date	Chapter	What is new
V1.00	2018-09-12		New version
V1.01	2018-09-19	2.1.1	1. SIM8950 Series I2C Driver Development Guide Manual

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This document describes the Inter-Integrated Circuit(I2C) and explains how to configure it in the kernel . Through these chapter , you can know to configure I2C.

1 Introduction

1.1 The Inter-Integrated Circuit(I2C) Overview

The I2C core supports I2C standard (100 kHz) and Fast (400 kHz) output clock frequencies. The MSM8953 chipset supports the following key features:

1. Enable Data Mover (BAM) integration
2. Support for I2C tag version

2 I2C Configure Process

2.1 Dts Configure

The steps required to configure and use any of the QUP cores that are available in the MSM8953 chipset as an I2C device are described below. By default, QTI has preconfigured BLSP1_QUP2 and BLSP2_QUP1 as I2C.

For more information, see:

- 1.Source code – arch/arm/boot/dts/qcom/msm8953-pinctrl.dtsi
- 2.Kernel documentation – Documentation/devicetree/bindings/i2c/i2c-msm-v2.txt

QUP Physical address

BLSP Hardware ID	QUP core	Physical address
BLSP 1	BLSP 1 QUP 1	0x78B5000
BLSP 1	BLSP 1 QUP 2	0x78B6000
BLSP 1	BLSP 1 QUP 3	0x78B7000
BLSP 1	BLSP 1 QUP 4	0x78B8000
BLSP 2	BLSP 2 QUP 1	0x78AF500
BLSP 2	BLSP 2 QUP 2	0x78 AF600
BLSP 2	BLSP 2 QUP 3	0x78 AF700
BLSP 2	BLSP 2 QUP 4	0x78 AF800

QUP IRQ

BLSP Hardware ID	QUP core	IRQ
BLSP 1	BLSP 1 QUP 1	127
BLSP 1	BLSP 1 QUP 2	128
BLSP 1	BLSP 1 QUP 3	129
BLSP 1	BLSP 1 QUP 4	130

BLSP 2	BLSP 2 QUP 1	331
BLSP 2	BLSP 2 QUP 2	332
BLSP 2	BLSP 2 QUP 3	333
BLSP 2	BLSP 2 QUP 4	334

For example, add a new one I2C2. First we need check hardware schematic and the I2C2_SCL、I2C2_SDA correspond to GPIO is GPIO6 GPIO7, So we only modify as below:

/kernel/msm-3.18/arch/arm/boot/dts/qcom/sim8950-msm8953.dtsi

```
i2c_2: i2c@78b6000 { /* BLSP1 QUP2 */
    compatible = "qcom,i2c-msm-v2";
    reg-names = "qup_phys_addr";
    reg = <0x78b6000 0x600>;
    interrupt-names = "qup_irq";
    interrupts = <0 96 0>;
    clocks = <&clock_gcc clk_gcc_blsp1_ahb_clk>,
    <&clock_gcc clk_gcc_blsp1_qup2_i2c_apps_clk>;
    clock-names = "iface_clk", "core_clk";
    qcom,clk-freq-out = <400000>;
    qcom,clk-freq-in = <19200000>;
    pinctrl-names = "i2c_active ", "i2c_sleep";
    pinctrl-0 = <&i2c_2_active>;
    pinctrl-1 = <&i2c_2_sleep>;
    qcom,noise-rjct-scl = <0>;
    qcom,noise-rjct-sda = <0>;
    qcom,bam-pipe-idx-cons = <6>;
    qcom,bam-pipe-idx-prod = <7>;
    qcom,master-id = <86>;
    dmas = <&dma_blsp1 6 64 0x20000020 0x20>,
    <&dma_blsp1 7 32 0x20000020 0x20>;
    dma-names = "tx", "rx";
};
```

2.2 GPIO I2C Configure

The documents we have to modify :

/kernel/msm-3.18/arch/arm/boot/dts/qcom/sim8950-msm8953-pinctrl.dtsi

```
i2c_2 {
    i2c_2_active: i2c_2_active {
        /* active state */
        mux {
            pins="gpio6", "gpio7";
            function= "blsp_i2c2";
        }
    }
};
```

```
};

config {
    pins= "gpio6", "gpio7";
    drive-strength=<2>;
    bias-disable;
};

};

i2c_2_sleep: i2c_2_sleep {
    /* suspended state */
    mux {
        pins = "gpio6", "gpio7";
        function = "gpio";
    };

    config {
        pins = "gpio6", "gpio7";
        drive-strength = <2>;
        bias-disable;
    };
};

};
```